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JANUARY 2006 | VOLUME 4 NUMBER 1

Incorporating XML and RSS at the device level

TECHNOLOGY FEATURE

PCI Express emerging as the interconnect standard

APPLICATION FEATURE

Innovative tools for multithread debug

PCI EXPRESS

Roundup of PCI Express standards

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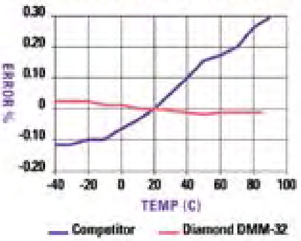

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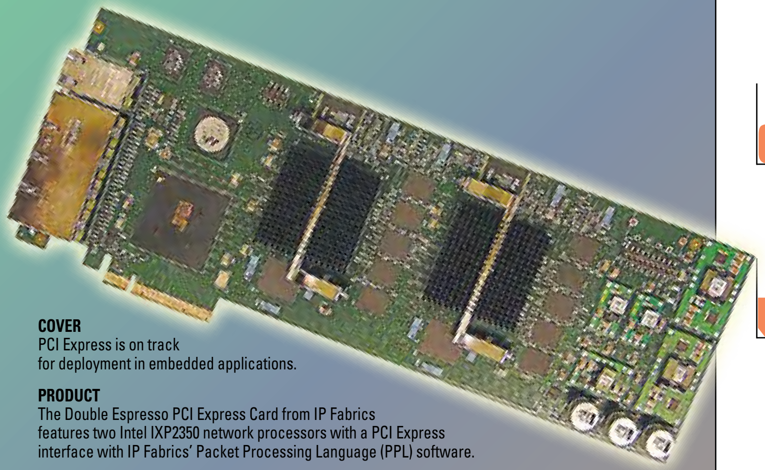

COVER
PCI Express is on track
for deployment in embedded applications.

PRODUCT
The Double Espresso PCI Express Card from IP Fabrics
features two Intel IXP2350 network processors with a PCI Express
interface with IP Fabrics' Packet Processing Language (PPL) software.

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CORRECTION: The November 2005 issue of *Embedded Computing Design* article entitled "Creating fast bit-accurate fixed-point simulation models in MATLAB for accurate verification and prototyping of signal processing algorithms" by Anu Shivaprasad of Catalytic Inc., contained incorrect headings on Figures 2 and 5. They should have read "Performance curves for 12 Mbps 802.11a Link (10000 MAC frames)." OpenSystems Publishing regrets the error.

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The embedded computing market

Jerry Gipper

I often struggle with the definition of "embedded computing," so I recently went to Wikipedia.org to see what they had to say about it. I entered "embedded computing" into their search engine, and was promptly redirected to "embedded system." At first I thought that was odd, but after reflecting for a moment, I realized that what we are really talking about in the embedded market is a complete system. So maybe "embedded system" is very appropriate.

Wikipedia defines "embedded system" as: *A special-purpose computer system, which is completely encapsulated by the device it controls. An embedded system has specific requirements and performs predefined tasks, unlike a general-purpose personal computer. An embedded system is a programmed hardware device. A programmable hardware chip is the "raw material," and it is programmed with particular applications. This is to be understood in comparison to older systems with full functional hardware or systems with general-purpose hardware and externally loaded software. Embedded systems are a combination of hardware and software, which facilitates mass production and variety of application.*

This definition suits *Embedded Computing Design* very well. The products that go into making this "embedded system" are exactly what we are striving to cover. The range of applications includes pretty much everything except personal computers and servers.

In future columns, I will go more into this definition, market trends and related business topics.

The January issue of *Embedded Computing Design* sees us launching a new section that focuses on PCI Express technology and products. Future issues will continue to include this section, as we plan to cover a range of PCI Express-related topics including intellectual property, chipsets, modules, backplane implementations, software, and development tools.

In this issue we will be covering:

Structuring embedded software

- *Incorporating XML and RSS at the device level*, written by Andrew Corlett of Lantronix. XML and RSS are becoming familiar to all of us. Andrew looks at how embedded devices can start to use this technology to communicate between themselves and real-time databases. He gives us a better understanding of what RSS can do in embedded applications.

PCI Express – Current state of affairs

- *PCI Express emerging as the interconnect standard*, authored by John Gudmundson of PLX Technology. John shows us how PCI Express leverages the extensive amount of PCI bus legacy software, how designs can migrate from PCI bus to PCI Express, and what types of activities are going on with PCI Express in embedded applications. He closes with a summary of what we can expect in the coming years.
- *Platform ASICs provide PCI Express alternative*, composed by Greg Martin and Grant Lindberg of LSI Logic and Jusak Effendy of GDA Technologies. There are multiple options for developing digital designs with a PCI Express interface. The LSI Logic team outlines the choices along with the pros and cons of each. They discuss the key considerations that should be examined before making a choice.
- *Wanted: Higher bandwidth, greater flexibility*, penned by Robert Hollingsworth of SMSC. Robert provides us some great insight into what is keeping PCI Express from busting out into widespread implementation in the mass markets. He takes a look at the current state of affairs and makes predictions on when PCI Express devices may become ubiquitous.

Multicore, multithread testing

- *New intelligent multithread processors benefit from integrated and innovative tools for code debug, programming, and test*, by Bob Burrill of Corelis. Multicore microprocessors architectures with multithreading are quickly being rolled out by all of the major microprocessor suppliers. The development environment around these chips has moved up to a new level of complexity, but the reasons for using the new architecture are so compelling that multithread processors are sure to grow quickly in application. However, the complexity of these parts does not make it an easier to test and debug. Bob discusses the advantages of the multicore, multithread architecture and looks at what tools are doing to keep up.

PCI Express – Modules

- Many older form factor modules are adopting PCI Express, and a wealth of new modules is also emerging. I will analyze the trends in pluggable modules that use a PCI Express interconnect and give you some idea of what to expect in the future.

Our 2006 editorial calendar is now online where you can see what topics we plan to cover throughout the year. We will continue to cover technologies of all types that impact your embedded computing designs, plus explore software and customization in embedded computing. We are always seeking interesting application stories that show how embedded computing is changing our lives and ways of doing things.

Your suggestions and comments are welcome. Please contact me at jgipper@opensystems-publishing.com.

Gerald J Gipper

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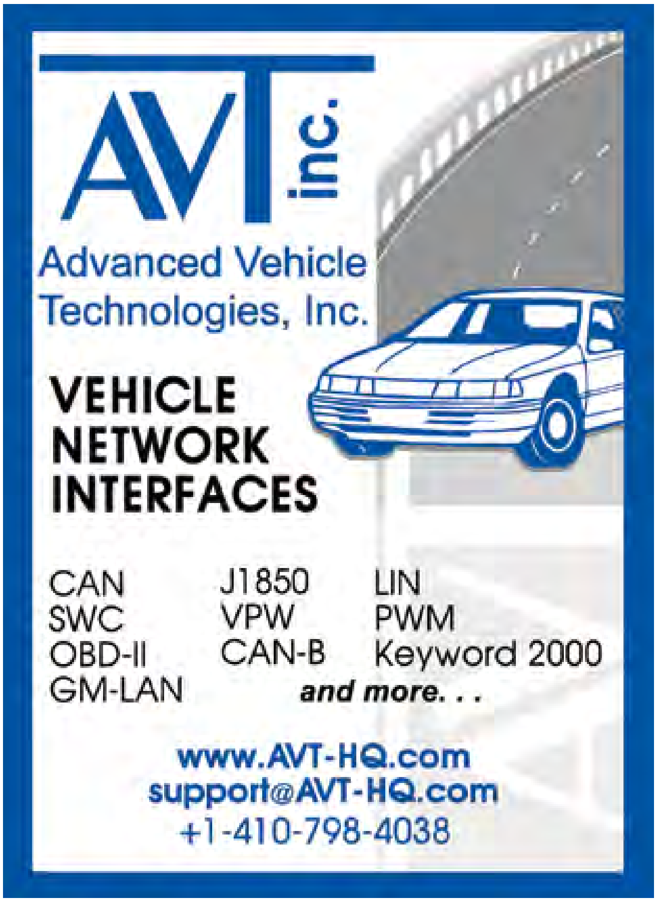
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By Don Dingee

Change takes more than a memo

We hear this phrase *sea change* touting a sweeping transformation about to take place that we all should be breathlessly awaiting. The phrase invokes a cultural reference to Shakespeare's *The Tempest*, and when used by an industry thought leader, it's all but guaranteed to generate media coverage.

But in fact, change is a complicated process and is rarely sudden, total, or even well marked at the time. Pri Shah and Diane Selleck at the University of Minnesota suggest that in order for change to occur, three *threads* must be dealt with and aligned for success.

- **Technical:** While many important technologies are invented, most changes come through innovation using available technology.
- **Political:** An urgent and important need must exist, and the power structure (management, industry, government, or society – whatever level applies) must at least allow, but preferably support, and even better embrace, change.
- **Cultural:** Change must be observed by others, deemed useful, and tried, implemented, adapted, and ultimately widely accepted.

We'll look at two examples of change spearheaded by technological innovation that impacted their spheres of influence, and some of the technologies poised to drive new change.

Video assist for the zany

It's January 1960. In exchange for Paramount's commitment to move *Cinderfella* back to a winter holiday release, Jerry Lewis commits to deliver an alternative summer movie to fill the gap. The problem is Lewis doesn't have a movie ready, and is booked for his night club act in Miami and Las Vegas over the next several months. Unfazed, he sets out on his own as producer, writer, director, and actor, and conceives *The Bellboy* around Miami's Fontainebleau Hotel where he is performing next. He takes a novel, creative approach in his script, departing from a linear narrative in the story and using location shooting exclusively, but also looks to technology to help meet the tight deadline he faces.

To speed production, Lewis turns to a new innovation he and a team at Paramount had been working on for about four years, formally called *Closed Circuit Television Applied to Motion Pictures*, which we know today as video assist. Video assist uses a bore-sighted video camera mounted on the film camera to record and display the scene on an attached television monitor, enabling the director and crew to watch the scene unfold and alleviating the need to develop film for daily proofing of footage.

By using video assist, Lewis was able to review shots immediately, and in many scenes was even able to turn the monitor toward the actors including him to help with positioning. Using this new tool for the first time, Lewis writes and shoots all footage in an unheard of 26 days during February and early March, and edits the finished 72-minute movie during his subsequent stay in Las Vegas. *The Bellboy* is released as planned that summer. Though critically panned, the movie becomes a box office hit and Lewis' most profitable film (since it was self produced and very inexpensive to shoot), and propels him to even bigger success in the next several years.

Lewis continued to use and enhance video assist in his next projects. Cinematographic purists resisted adopting it, but studios saw the productivity improvement and started to drive its acceptance. Video assist techniques became part of most directors' routine process over the next several years. Outside of the patent he received, praise from his inner circle, and adoration from his fans, Lewis never gained widespread recognition for this breakthrough innovation that changed the motion picture industry.

A very heavy inventory problem

One of the primary lessons from the 1991 U.S./Iraqi Desert Storm conflict was the impact of *smart bombs* – guided weapons that greatly increased bombing accuracy and dramatically reduced requirements for

> "…the stable technology of video cameras, TV monitors, and GPS intersected with the political and cultural climate of the respective time to drive change.

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sorties and ordinance drops. The U.S. Air Force could not get enough of them, but they were very expensive in the mid-1990s. Even worse, the Air Force had a huge inventory of *dumb bombs*, conventional unguided freefall weapons for large-scale use such as high altitude B-52 raids.

What if a way could be found to convert a dumb bomb into a smart bomb? Again, available technology meets innovation in the solution: Joint Direct Attack Munition (JDAM), developed by a team at Boeing (formerly McDonnell Douglas) and first operational in 1997. JDAM takes widely available GPS technology along with an Inertial Navigation System (INS) and builds it into a bolt-on, field-installable conversion for a variety of conventional unguided bombs. Units have been produced at less than half of the original cost estimate, further saving taxpayer dollars. The fins were borrowed from a sheet metal supplier to Toro for lawnmowers, rugged plastics were borrowed from the automotive industry to house the electronics, and the rest consists of a 24 MHz CPU, a cost-effective INS, a GPS receiver, and an electric motor driving the fins.

JDAM creates accurate, all-weather, independent targeting capability and enables dispensing as far as 15 miles from the target – truly a force multiplier for mission planners. A single B-1 can carry 24 of the 2,000 lb variety, programming the units in the air with fresh targeting information right up until dropping them. John Pike of the Federation of American Scientists said about JDAM's impact, "It's right up there with the machine gun and the atomic bomb." Pike also said one Navy admiral has credited the JDAM with increasing the lethality of an aircraft carrier fivefold.

The next wave

In these examples, the stable technology of video cameras, TV monitors, and GPS intersected with the political and cultural climate of the respective time to drive change. What embedded technologies are closing in on having all three threads – technical, political, and cultural – to create a significant change in how things get done? Here are some I see:

- **Flash memory:** After years of development and improvement in cost and reliability, flash has already had a dramatic impact on handheld devices and now appears poised to deliver a knockout punch to rotating storage single drive applications in the next couple of years.
- **Ajax programming:** Creating Web applications with two solid technologies, asynchronous JavaScript and XML, Ajax is starting to gain acceptance with interactive developers such as the teams at Google who produced Google Maps.
- **Virtual simulation:** Cycle-approximate simulation of microprocessor devices is allowing software teams to develop and evaluate earlier in the development cycle, increasing code quality and reducing development time.
- **FPGAs:** Improvements in speed, density, and easier-to-use development tools coupled with reductions in cost have FPGAs gaining wider and wider acceptance, especially in signal processing applications.
- **Open source software:** Whether it is Linux, Eclipse, or other technology, open source software allows companies to move more quickly to adding value and solving difficult problems by building on a stable base of code.
- **Wireless networking:** With Wi-Fi and Bluetooth having found places already, the next standards to pick up should be ZigBee, followed by the intermediate range WiMax, which opens up a new class of applications.
- **Multicore processors:** Vendors are just starting to exploit uses for multiple cores, and one emerging potential is for energy reduction using fewer multicore-based servers compared to an equivalent number of single core servers, a politically attractive angle.

More than just technology and a memo

We have a great range of embedded technology to work with today, but creating real change takes more than just having the technology and issuing a memo or a press release. It takes being faced with a need, having the innovative talent to fill it creatively with available technology, and helping others realize the same benefits on a wide scale. Give this some thought within your company as you look to make that next breakthrough, and maybe historians will look back upon your efforts as a *sea change*.

As always, if you'd like to like to add your ideas to the discussion, I welcome your e-mails at ddingee@opensystems-publishing.com. Here's to a great 2006 for all of us.

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Embedded electronics in helicopters

By Hermann Strass

Eurocopter (Germany, France), an EADS company, announced the "world's quietest" helicopter on September 8 at their main German factory and headquarters in Donauwoerth, Germany. This achievement, after nine years of research, is very significant in itself, but also because it was achieved using many embedded electronics.

Especially during takeoff and landing, helicopters make a loud noise similar to a rapid succession of whipping sounds. This is the result of air turbulence at the trailing edge of the rotor blades. Small air bubbles form there, and the next rotor blade literally cuts these air bubbles as it moves around. This effect not only produces noise, but it also reduces the power and fuel efficiency significantly. Commercial jet aircraft cut this turbulence by placing small rectangular blades (like cards in a card game) vertical onto the upper edges of the wings.

Eurocopter has done research in cooperation with EADS, DaimlerChrysler, and DLR (see *VMEbus Systems*, August 2005, available at www.vmebus-systems.com/columns/Technology_in_Europe/2005/8/), all in Germany, to solve the noise and performance problem. Very fast electronic control modules influence the angle of the rotor wing edges (vortices) by piezo-electric action (up to 40 times per second). This goes well beyond traditional flap control. Embedded electronics control this fully automated adaptive rotor system, and the pilot does not need to do anything. Figure 1 depicts Eurocopter model EC145, the successor to model BK117, which was used most of the time during the development of the embedded-control intelligent adaptive rotor system.

An additional benefit of this real-time control is a significant reduction in vibration (up to 90 percent). This provides not only a more comfortable ride, but also increases the MTBF and performance parameters (speed, acceleration, flight, and distance). The noise reduction (up to 50 percent) and more comfortable ride are very important in air rescue missions and transport as passengers are subject to less noise and vibration. Eurocopter, which estimates that helicopters use more embedded electronics components per unit weight than cars or commercial aircraft, plans to significantly increase embedded electronics in helicopters in the future to improve performance, comfort, and economy.

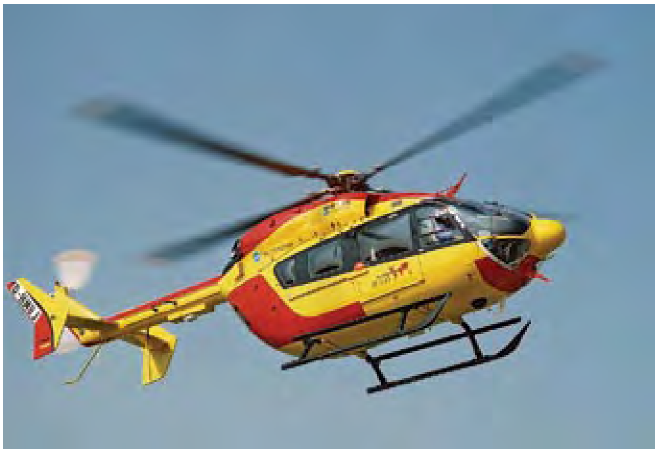

Figure 1

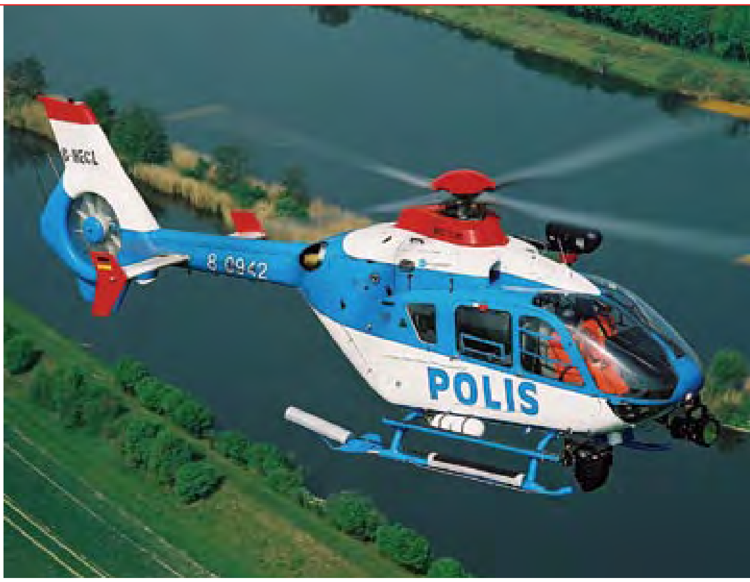

Figure 2

The American subsidiary of Eurocopter, American Eurocopter, mobilized two helicopters, EC135 (Figure 2) and EC120, with American pilots within hours of Hurricane Katrina's passage. They carried medical supplies and medical technicians into the ravaged regions of Louisiana and Mississippi and transported infants requiring medical attention from New Orleans to outlying medical facilities. They also rescued 66 people from the roof of Tulane University in New Orleans. Later missions were concentrated on supply and rescue flights along the Mississippi coast. Three American Eurocopter corporate customers also volunteered to assist in this humanitarian effort.

Research

The European Union (EU) puts a top priority on the technology platform Artemis for Embedded Systems, the fastest growing IT sector. The EU will subsidize this project with € 640 million (approximately U.S. $754 million) from now until the year 2015. Leading European electronic enterprises cooperate under EU supervision (public/private partnership) to generate a strategic agenda, standards, and compatibility for embedded systems, and link with initiatives outside the EU.

According to an Artemis press release, "Embedded systems are virtually invisible by the user. About 98 percent of today's computing devices are in embedded systems – not in PCs – and their number is expected to exceed 40 billion devices by 2020. In Europe, the number of people developing embedded systems is estimated at 150,000. This population is expected to double over a 10-year period." There are 11 projects out of 17 in the Sixth Framework Program of the EU that explicitly carry the term "embedded" in their title.

Learn more at their website www.cordis.lu/ist/embedded/.

Standardization

Electromagnetic interference and compatibility are a big problem in this electronic age. The purpose of the European Norm EN 50366 is to limit the electromagnetic fields produced by electrical household appliances in order to protect human beings, animals, and plants. This norm is about *Electromagnetic Fields Compliance* (EMF), such as possible irritation of muscles and nerves, shock, burns, insomnia, or increased temperature of tissues. It provides a method to prove compliance with EU directive 1999/519/EG and low-voltage directive 73/23/EEC. It will become mandatory in February 2006, and it is one of the requirements to allow a company to put the CE mark on their products.

> "The trends include a shift to more nonvoice services, more user-friendly devices, and more mature content services.

Kontron (Germany) has developed and presented the E2Brain Computer-On-Module (COM) specification in 2002. They are now offering this specification for download at www.e2brain.com/specification.pdf. Kontron plans to create a consortium around this specification. They currently offer six different evaluation kits for various microprocessor platforms.

Business

European revenue from mobile Location-Based Services (LBS) will more than double in 2006, according to telecommunications industry research firm Berg Insight (Sweden). This year the growth rate is estimated to be 153 percent (to € 274 million) and annual growth rates of 84 percent are expected over the next five years. The trends include a shift to more nonvoice services, more user-friendly devices, and more mature content services. Mobile phones with integrated GPS navigation from Vodafone and TeliaSonera are examples of these trends. Tracking the position of employees, vehicles, or other movable assets can improve efficiency as well as maintain a higher level of security, like retrieving valuable cargo from stolen vehicles.

BuS Elektronik (Germany) received the "Best Factory/Industrial Excellence Award" on September 27 in Nuernberg, Germany. BuS Elektronik is a medium-sized Electronic Manufacturing Services (EMS) company (see *CompactPCI & AdvancedTCA Systems*, May 2005, available at www.compactpci-systems.com/columns/Technology_in_Europe/2005/5/) that has grown in 10 years from € 7 million to € 56 million (approximately U.S. $8.2 million to $66 million) and now employs more than 450 people. They have received "excellence" marks in the categories of operational strategy, product development, and continued improvement processes. The jury consisted of experts from the highly reputable INSEA management institute in Fontainebleau, France, and from the WHU, Scientific University of Corporate Management, in Germany. BuS Elektronik is based in Riesa, Saxonia, only a few miles away from the Silicon Saxonia region in and around Dresden where companies like AMD, Infineon, Wacker Silicon, and others produce some of the most advanced memory and microprocessor chips.

Future development

The Emirate of Dubai has created the Dubai Silicon Oasis (DSO) as a rival to U.S. and Asian centers and to complement the Silicon Valley in California. This is one of the efforts to plan for economic development after oil runs out. The DSO will initially cover about 7.2 million square meters (approximately 77.5 million square feet). Business-ready facilities support the DSO's world-class infrastructure, and the DSO cooperates with leading technology providers. Equipment for chip design, development, and production, with emphasis on mixed-signal, RF/analog, and similar embedded markets, is ready for use. The DSO claims all you need is a product idea; everything else, including the latest EDA tools and IP libraries, is already available. The government of Dubai is very cooperative, such that a new enterprise might be able to get started within about 30 days.

The DSO, a member of SEMI, FSA, and SIA, has started business this month under the direction of Dr. Juergen Knorr, a former top manager and CEO of Siemens Semiconductors (Germany). The Analyst International Data Corporation expects that the United Arab Emirates (UAE), including Dubai, will invest about € 6.6 billion (approximately U.S. $7.8 billion) in 2006 to participate in a market that IC Insights expects to reach 900 billion in 2007. Companies like Synopsis and EtherCom (both United States) or The Time Group (UK) have started or announced presence at DSO. The government of Dubai protects Intellectual Property (IP) with the most stringent IP and copyright laws.

Apart from electronics, Dubai has invested heavily in attracting money-spending tourists by building one of the world's most luxurious hotel and three gigantic artificial islands. The third one is a complex of 300 mini islands that look like a map of the world from above.

Events

Every odd-numbered year, Berlin is the site of the Internationale Funkausssstellung (IFA), which is the world's largest event for professional entertainment technology. More than 1,200 companies from more than 40 countries showed their products September 2-9 to about 250,000 professional experts.

The Games Convention (GC) in Leipzig, Germany, August 18-21 last year had record attendance of more than 134,000 games designers, developers, and producers, an increase of 27 percent over attendance in 2004. Europe's largest event of this kind also attracted about 2,000 journalists. Participation at the parallel event, Games Convention Design Conference, doubled in comparison to the previous year. The business section of the GC, which is off-limits to the general public, doubled in size over the area in 2004. As a consequence of the success of the GC in Leipzig, the association of British games publishers cancelled their event, *European Games Network* (EGN), and another former European event, ECTS (London), was also cancelled.

Both events, IFA and GC, represent a significant market for embedded computing design and products.

Eclipse for embedded targets

By Gene Sally

As readers of this column are well aware, Eclipse is a general-purpose application development platform incarnated as an IDE. While first introduced as a Java IDE in November 2001, the C Development Tools (CDT) team shortly followed that release with the first installment of the C/C++ development environment.

One segment of the market that quickly adopted Eclipse was the embedded tools market. Prior to the rapid adoption of Eclipse, all of the vendors in the embedded market maintained their own IDE distributions. However, the open nature of the Eclipse framework and surrounding plug-ins made it a natural choice for those who wanted to just concentrate on the value-added features for embedded developers, namely:

- Cross-compilation
- Remote debugging
- Target management
- Target configuration

Code development for an embedded target shares many of the same IDE features as any other coding project. From the perspective of the user, these are low-valued features. Having them work well is vitally important, but the user just expects the editor to contain all of the bells and whistles found in the hundreds of editors already in the market.

Likewise, the user of an IDE expects the project management functions just to work, and consequently does not view them as highly valuable features of the product. The large amounts of effort required to get these features working takes resources away from the goal of producing the specific requirements of embedded engineers. Furthermore, the engineering costs for making the things that should "just work" must be amortized over a smaller user base, driving up the costs and pricing of tool products.

Device coding projects

With the introduction of Eclipse and the CDT, companies in the embedded tools space found the solution to their problem of delivering a high quality IDE experience to their users while delivering the embedded developers specialized tools. Eclipse and CDT handled the C/C++ development toolset, granting the embedded tools vendor the bandwidth to focus on just the small slice of features required by their users.

As embedded tools vendors worked on their products, it became apparent that many were still solving problems common to all vendors in the market. For example, when TimeSys launched TimeStorm IDE three years ago, it contained plug-ins for cross-compiler support, remote execution/debugging, and target management. Other IDEs from companies in the market followed suit, each with their own plug-ins solving similar problems.

The open, plug-in-oriented nature of Eclipse made it possible for embedded vendors to work on creating plug-ins for these common requirements as well. To reach that goal, the Device Software Development Platform (DSDP) project was proposed and subsequently approved by the Eclipse board of directors June 8, 2005.

The DSDP project charter states: "The Eclipse Device Software Development Platform Project is an open source collaborative software development project dedicated to providing an extensible, standards-based platform to address a broad range of needs in the device software development space using the Eclipse platform."

The project, currently led and staffed by engineers from Wind River Systems, is working toward creating solutions for target management and device debugging.

DSDP target management

Embedded engineering typically means developing code that will run on a target other than that of the development host. The target management project will focus on integrating that interaction into Eclipse by allowing the user to define remote targets and the preferred method of communication. The project aims to provide management and communication to a wide range of devices, from FPGAs attached to a hardware debugging device to a full-blown Linux distribution running *ssh* daemons.

Once a communication channel has been established with the device, the target management project will also cover how to manage the device by being able to query its state and starting and stopping processes, services, and cores. These features will afford the engineer complete control over the target from within the Eclipse environment.

This month, the target management group anticipates the open source release of the IBM Remote System Explorer (RSE) plug-in, which has been deployed to IBM customers the past four years. The RSE will allow users to inspect running processes, upload/download files and inspect a Linux target's file system. The RSE's data model will serve as the foundation for additional systems supported by the tool in the future.

Subsequent milestones for the target management project in summer 2006 are to build a remote launch facility that leverages the infrastructure and data model exposed by the RSE, as well as that of the device debugging project.

DSDP device debugging

Even the best coders spend most of their time debugging. Vendors in the embedded space that support remote debugging within Eclipse do so by taking advantage of the existing local debugging code base, then adding code that initiates a remote connection during the phase where the underlying debugger (typically GDB) starts. Once GDB starts, it supplies the information used by Eclipse to render the views in the user interface, and the user is presented with the same interface as used for local debugging.

While this approach provides a good user experience, it suffers from some limitations. For example, a user cannot attach to a running process on the target, nor can the user have more than one debugging session running at a time. In addition, the user interface doesn't efficiently collect the necessary data to populate the views, meaning slower performance as the low-bandwidth connection to the target is taxed gathering data to drive the display.

To address these issues, the device debugging project is first reworking how the underlying debugging interfaces in Eclipse work to better accommodate embedded engineers. The device debugging team has developed a set of prototype interfaces that allows views to have their own update policies, allowing each view to have a different update policy to match the data displayed and the capabilities of the remote target. Due to the complexity of the proposed solution and the coordination efforts between the CDT and DSDP teams, expect to see these features starting to appear this summer.

Conclusion

Eclipse has gained momentum in the embedded market, and the DSDP project is now busy tackling the issues salient to embedded engineers and the vendors supplying them tools. This year promises great advancements in the Eclipse project for embedded engineers and will lay the foundation for continual improvements in the years to come.

Gene Sally *is product manager for TimeSys LinuxLink. Gene has been working with Linux for eight years, five of those in an embedded environment, and has been using Eclipse since beta.*

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Incorporating XML and RSS at the device level

By Andrew Corlett

As Extensible Markup Language (XML) and Really Simple Syndication (RSS) are becoming more widely accepted as standards for configuration, control, and information transport, embedded applications are beginning to exploit and revolutionize the capabilities of these protocols at the device level. Now, networked devices are able to communicate with these business and Internet protocols, enabling rapid integration of device information into mainstream enterprise IT applications. A corporation's device assets are now capable of real-time delivery of business-related information to "information consumers" within the organization.

Though the ability to utilize XML and RSS in embedded systems presents huge potential for designers, it is important to fully understand their capabilities and what is required to incorporate them into a design. This understanding begins with a study of how these protocols differ, what each offers, and how they can work together to provide a more flexible and effective means for transferring and collecting information.

Understanding XML

XML is a method that allows different devices, systems, or machines with a variety of data command and control structures to communicate with each other. This protocol offers the potential to alleviate many of the interoperability problems associated with the sharing of documents and data from a variety of sources. It allows information and services to be encoded with meaningful structure and semantics that both computers and humans can understand. XML is an ideal protocol for information exchange and can be easily customized with user-specific and industry-specific tags. It provides a flexible means to establish common information formats and to share both the format and the data.

Organizations that collect RFID data may find XML and possibly RSS (a lightweight XML format designed for sharing, aggregating, and syndicating Web content) to be an effective method of storing RFID data into a remote database already in use by the organization. For example, XML and RFID together would enable a factory to store consumption rates of materials into a remote database. Using RSS, this data can then be easily shared with key personnel who can place materials orders and conduct operational analyses from any location in real time. RFID technology will provide a new dimension to data and better accuracy of data collected. Since databases use XML, it can be very simple for an XML-enabled RFID reader to store data directly into a corporate database.

XML uses text as its character set, a common language all computers and computing devices can process. Because XML offers unlimited flexibility in structuring data, different devices can be equipped to communicate with each other quite easily. XML is rapidly growing in popularity because of this ease of use and flexibility, and this in turn makes it easier for designers and engineers to interface their devices and applications.

RSS complements XML

The technology behind RSS is well tested, having emerged from Netscape in 1999. RSS is a widely adopted XML format that describes a channel of information. Information within a channel is grouped into individual *items*, each containing required

XML and RSS

elements such as a title, description, and link that leads back to the original information, in addition to other optional elements such as a timestamp. Figure 1 shows an example of an RSS code.

Typically an RSS XML document (or database output) is hosted on a Web server and retrieved by an RSS reader (sometimes called an aggregator; see Figure 2 for an example). A device server with Web server capabilities is therefore able to create an RSS information channel, also known as an *RSS feed*, and broadcast information, such as device performance data, to any number of users.

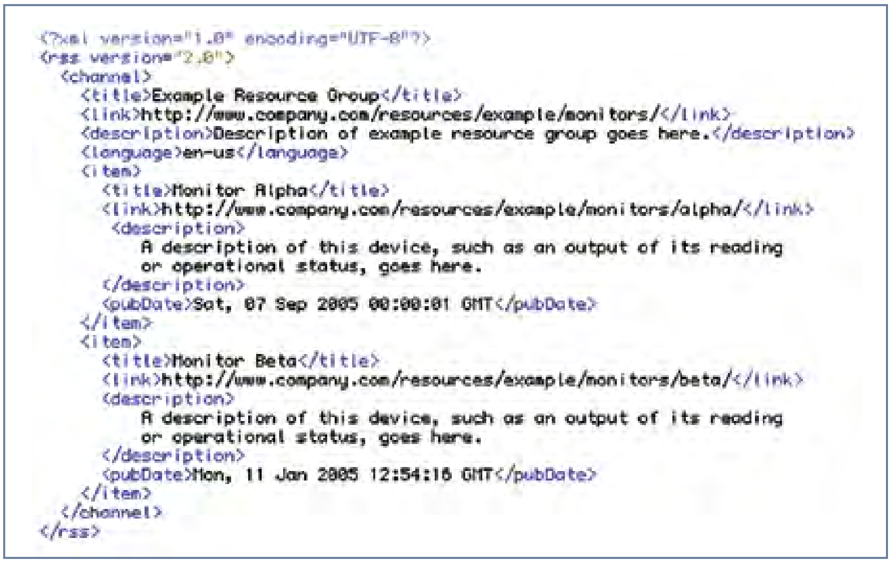
Microsoft's Internet Explorer version 7.0 will include a built-in RSS reader. Other browsers – Mozilla's Firefox and Opera – already offer RSS as a standard add-on. Standalone RSS readers are also available.

RSS aggregators are readers enhanced with the capability of bringing together multiple RSS feeds in one location. An aggregator can be scheduled to periodically check RSS files in the user's list to determine whether new content has been added. Some programs notify users with alerts and flags when changes within the RSS feeds are detected.

The simplified gathering of data by RSS readers enables users to correlate multiple channels of information, a capability not offered by simple e-mail alerts. In addition, RSS adds intelligence to networked devices providing a means for users and managers to quickly analyze a system of diverse devices.

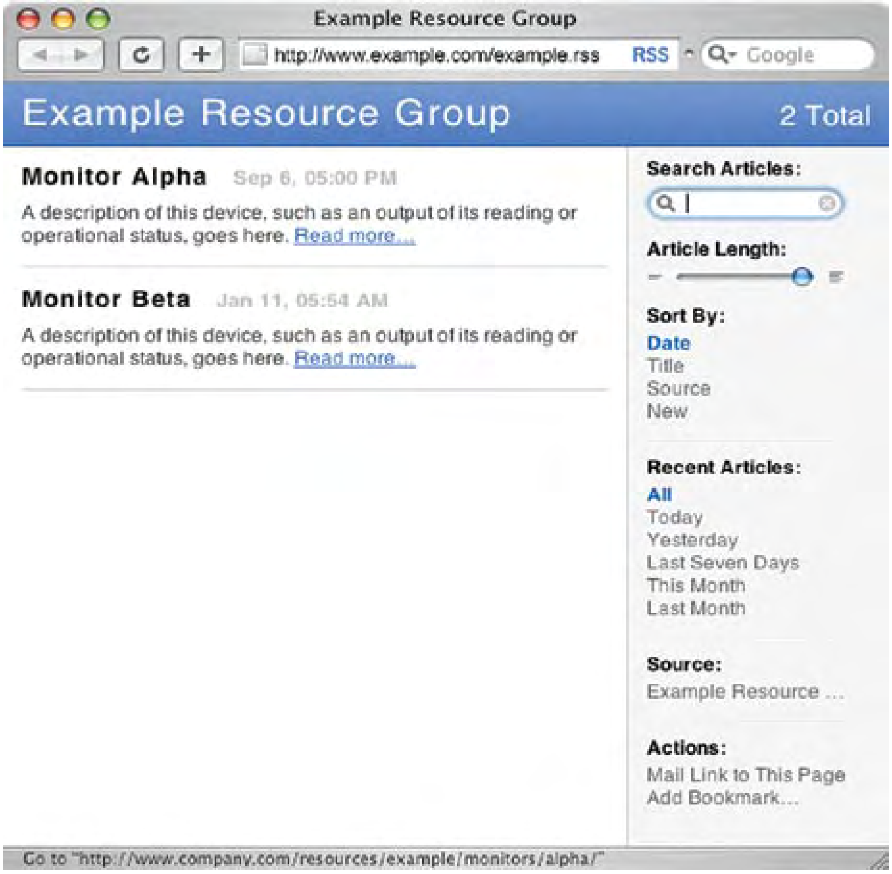
For embedded designs that include a variety of systems and hardware, XML is an absolute necessity, and RSS provides an ideal method of disseminating XML data for human readability and usability. Together, XML and RSS provide more flexible and effective methods of exchanging data in human-readable, human-useable formats and for Machine-to-Machine (M2M) communication, facilitating the distribution of business logic to a variety of systems.

Devices can now provide the ability to have their information retrieved by RSS aggregators as well. For example, a factory's temperature readings can be sent to an RSS aggregator for a manager to monitor and control. In an office security system, monitoring devices send their XML to a database for storage or to an application, which may autonomously decide when to call the police or fire department. If office managers need to see the data as well, they can use RSS to retrieve it from anywhere.



```
<?xml version="1.0" encoding="UTF-8"?>
<rss version="2.0">
  <channel>
    <title>Example Resource Group</title>
    <link>http://www.company.com/resources/example/monitors/</link>
    <description>Description of example resource group goes here.</description>
    <language>en-us</language>
    <item>
      <title>Monitor Alpha</title>
      <link>http://www.company.com/resources/example/monitors/alpha/</link>
       <description>
          A description of this device, such as an output of its reading
          or operational status, goes here.
      </description>
      <pubDate>Sat, 07 Sep 2005 00:00:01 GMT</pubDate>
    </item>
    <item>
      <title>Monitor Beta</title>
      <link>http://www.company.com/resources/example/monitors/beta/</link>
      <description>
          A description of this device, such as an output of its reading
          or operational status, goes here.
      </description>
      <pubDate>Mon, 11 Jan 2005 12:54:16 GMT</pubDate>
    </item>
  </channel>
</rss>
```

Figure 1



Example Resource Group 2 Total

Monitor Alpha Sep 6, 05:00 PM

A description of this device, such as an output of its reading or operational status, goes here. Read more...

Monitor Beta Jan 11, 05:54 AM

A description of this device, such as an output of its reading or operational status, goes here. Read more...

Go to "http://www.company.com/resources/example/monitors/alpha/"

Figure 2

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Managers can use one aggregator to gather RSS data from 100 different offices; one RSS aggregator, for example, may be used to check the open/close status on all 100 doors. XML and RSS can also be used together for mailing services such as UPS. XML is used to transmit the status of a package to a corporate data system, and then RSS is implemented to feed the package data to the end customer.

Integration basics for both protocols

Integrating XML and RSS into an embedded design can be challenging for designers who are not familiar with them. It is imperative to understand the basics of implementing the two protocols before attempting integration.

A basic infrastructure that includes a transport mechanism, files, and memory must be in place to support both of these protocols, since RSS requires XML to transport form to function. The transport mechanism allows for M2M and application-to-application communication using HTTP, TCP/IP, and other protocols. The system must have the ability to store files as well as configure information and command history. This file system must be capable of supporting FTP, TFTP, Web, and command access, and requires a protocol stack. Passed-in memory is necessary to allow for the ability to communicate application-to-application on the same system.

Currently, there are integrated solutions being developed that allow embedded designers to quickly and easily add these functions and capabilities to their applications. Such solutions eliminate guesswork on the part of designers and facilitate a faster design cycle.

Showing promise well into the future

Together, XML and RSS can add substantial value to a variety of applications, including but not limited to factory automation, health care, and a growing M2M segment.

The convergence of machine information with enterprise business processes is expected to transform the way companies operate and deliver services. M2M integration adds tremendous value by enhancing processes such as workflow, asset tracking, customer service, and product maintenance in a wide variety of vertical markets including industrial and building automation, security, health care, finance, energy metering, and retail.

As more and more enterprise users need to access data from a multitude of devices and locations, we can expect that XML and RSS will become increasingly ingrained into business IT structures stretching all the way to edge devices to deliver on the promise of the "real-time" enterprise. **ECD**

***Andrew Corlett** joined Lantronix in 2002 and is currently a principal engineer there. With more than 10 years of successful software and hardware project management and development experience, Andrew is the author of three patents and an originator of a number of products. Andrew holds a BA in Computer Science from the University of California, Berkley.*

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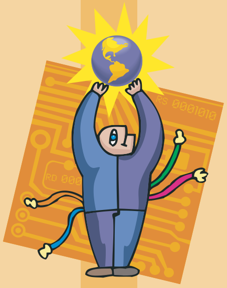
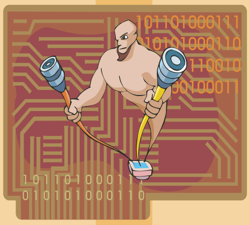
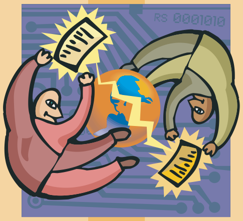
PCI Express – Current state of affairs







PCI Express emerging as the interconnect standard

By John Gudmundson

PCI Express (PCIe) technology is now emerging as the interconnect standard for both chip-to-chip and backplane-interconnect designs, with broad applicability in PCs, servers, communications, storage, and embedded systems. Unlike several other potential interconnect solutions, it is based on the ubiquitous PCI bus specification and allows for extensive reuse of existing PCI software. PCIe is distinct from the 32-bit PCI and 64-bit PCI and PCI-X shared parallel buses (collectively PCI/X) by providing a high-performance serial, packet-based, scalable architecture designed to overcome the limitations of PCI/X, dramatically improve time to market, and deliver new standardized features. PCIe switches provide standardized solutions utilizing existing code yet allow advanced system designs to be developed.

PCI, PCI-X interconnect limitations

Currently, many backplane designs use PCI/X as the interconnect technology. PCI bus is limited in throughput to one gigabit per second (1 Gbps) and involves a shared multi-drop bus. With its multiplexed address and data, PCI is slowed by wait states added by both master and target devices. As data transfer sizes are unknown at the start of a burst cycle, PCI buffer management is highly inefficient. With no split-level data transfers, delayed transactions are also inefficient since the master must guess when to attempt retransmissions. With a shared bus such as PCI/X, interrupt signals may come from a variety of devices, so additional software overhead is needed to determine which device generated the interrupt. When parity or other errors are detected in PCI, an interrupt occurs and causes a system shutdown, for which no error detection and recovery is provided.

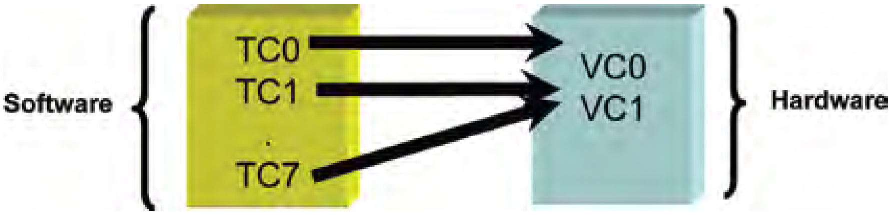


Figure 2

PCI-X was developed as a speed enhancement to PCI and has been designed into servers, communication solutions, and, more recently, embedded systems, and is fully backward compatible with PCI at both the hardware and software levels. With PCI-X 2.0 and its double and quad data rate clocking modes, data rates are able to reach 32 Gbps. PCI-X provides for several enhancements over PCI; PCI-X signals are registered (vs. unregistered for PCI), providing smaller setup time to sample a signal. Split transactions are employed, wait states are not allowed, data is transferred in blocks, typically 128 bytes in size, and most transfers are burst cycles, enabling higher bus utilization. The resulting data transfer efficiency approaches 85 percent, far higher than PCI's worst-case 50 percent. Other PCI-X advantages include more efficient interrupt handling with mandatory message-signaled interrupt support, improved error handling with attempts to recover data parity errors, and the addition of relaxed ordering capability. But despite these improvements, performance is not truly scalable, clock skew issues arise, fan-out limitations become severe, and board-layout space concerns occur at these large pin counts and higher frequencies. Yet, throughput demands march forward, beyond the scope of PCI-X. Neither PCI nor PCI-X supports peer-to-peer transfers without tying up the main bus; this prevents host-based services, thus causing a potential system bottleneck.

PCIe technology overcomes these limitations through scalable throughput and advanced features.

PCI Express: The new interconnect standard

In PCIe technology, the physical layer is based upon a dual simplex serial PHY and provides for switched point-to-point links, with only four wires per lane total, and no sideband signals. PCIe layout simplifies root complex chip designs, reduces the pin-out required, and allows more direct PCIe ports than does PCI/X. With the minimized routing, layout "hotspots" around the platforms CPU/memory/root complex can be avoided (see Figure 1). The fast/wide PCI-X traces can be moved to the board periphery with a 20-inch routing length permitted from PCIe root complex to PCIe bridge/switch devices. Clocking is embedded with the familiar 8 B/10 B encoding scheme. Each link can scale up to 32 lanes, and lanes transfer data at 2.5 Gbps in each direction for a potential total throughput of 160 Gbps. Future PHY layer enhancements will be boosted to 5 Gbps per direction per lane with scalability beyond this rate, while retaining the same higher-layer functions.

PCIe technology adds improved support for power management, hot plug, fault isolation, and error reporting. However, these enhancements don't conflict with PCI/X. For instance, PCIe bridges natively support hot plug on the PCIe side and through a Standard Hot Plug Controller (SHPC) on the PCI/X side. Power Management Events (PMEs) using the PME# signal are taken from the PCI/X interface of a bridge and converted to in-band PME messages on the PCIe side and routed to the system controller. Bridges use the PCIe Requester ID to identify the source of these PMEs. Bridges also support L0 and optionally L1 low-power states.

Beyond its speed and feature advantages over PCI/X, PCIe technology provides a rich new feature set, including quality of service, flow control, and peer-to-peer transfers that allow for usage in high-speed backplane designs, while maintaining backward-compatibility with PCI/X. With PCIe technology, data can be classified in up to eight classes and is invariant through the fabric. These Traffic Classes (TCs) are then mapped to multiple Virtual Circuits (VCs) in PCIe bridges and switches (see Figure 2). Each VC can in turn be assigned a priority level with various polling techniques to determine the next VC to transfer data. Each VC also will have buffer memory to prevent dropped packets; head-of-line blocking is nearly negated, and time-critical isochronous traffic such as audio and video can now be better supported.

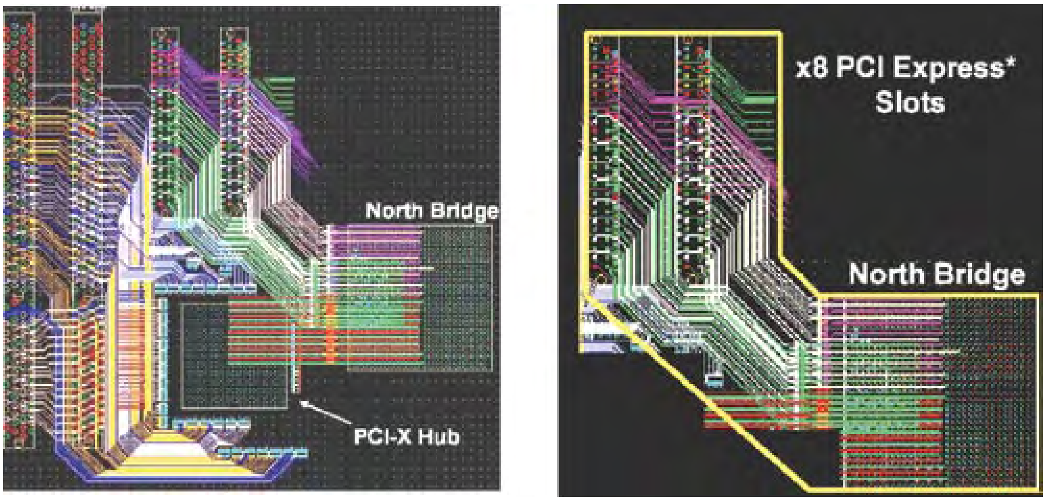


Figure 1

Flow control, which eliminates inefficient polling in PCI/X, is achieved through data link layer message transfers. In PCIe technology, flow control uses an input buffer, credit-based, per VC link flow control method. With this technique, for each VC, data is not sent to a device with input buffer memory that lacks sufficient space for a new packet; rather, data link layer flow control packets are sent to the sending node informing it of the amount of buffer space available. The nearest PCIe device can thus avoid congestion and potentially dropped packets. Peer-to-peer data transfers and message request transactions also are defined in PCIe for multiple hierarchies within a single fabric topology (see Figure 3). While enumeration of switches, bridges, and endpoints are host-based and routing is based on addresses, routing through the host is avoided.

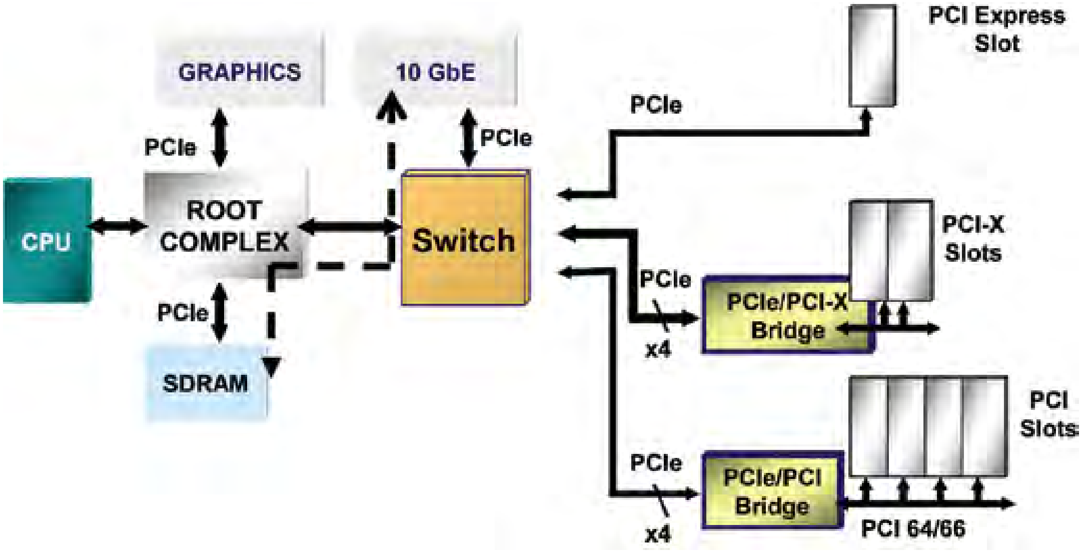


Figure 3

PCIe software compatibility with PCI/X

Just as existing code compatibility is a major determinant in the choice of a microprocessor for a given design, interconnect choices will need to factor in existing board subsections and add-in card device code. The programming model of PCIe software allows backward compatibility with PCI/X software. PCIe is also compatible with PCI/X at the hardware level, with PCIe bridges providing this backward compatibility at the component and slot level. During the transition to PCIe solutions, numerous endpoint devices and chip sets that utilize PCI/X will continue to exist. It is important from both time and cost standpoints that these chip sets, add-in cards, and other peripheral devices be supported.

PCIe software is backward compatible with legacy operating systems, drivers, and PCI software protocol stacks. The 256 byte base configuration address space for PCI/X is the same as for PCIe software, with this memory-mapped space extended to 4 kB for the added functionality associated with the enhanced features of PCIe technology. PCIe software reports class/subclass and device type information, just as in PCI/X. In transition from PCI/X to PCIe, memory, configuration, and I/O transactions are forwarded, and device ID message translation is optional. PCIe completion messages are translated to either delayed (PCI) or split (PCI-X) transactions, and locks are propagated. Data integrity is also supported through these bridges; on the PCIe side, link-level 32-bit Cyclic Redundancy Check (CRC) and optional end-to-end ECRC (generated at Layer 3) provide error checking. CRCs (16-bit) are also generated for messages sent at the data link layer. On the PCI/X side, parity and error checking and correction signals are generated. Errors occurring on the PCIe link can be propagated through the PCI/X side of the system for system controller software present on the PCI/X side. PCI/X interrupts are converted to PCIe assert/de-assert interrupt messages. Through reverse bridging, PCIe-based endpoints can be bridged to PCI/X-based systems, as well.

PCIe momentum

The first PCIe specification was released in April 2002 and since then has been revised twice, with version 1.1 finalized in April 2005. More than 500 companies now support the standard with silicon, software, test tools, IP, and programmable devices. The silicon covers the gamut, from north bridges to switches, bridges, and endpoints for PCI/X, gigabit Ethernet, and InfiniBand. A complete ecosystem is now in place with five specifications released to help with testing and interoperability assurance.

PCIe-enabled personal computers with enhanced graphics are already on the market. Many server designs are transitioning to PCIe technology, with storage systems following right behind. With PC, server, and storage designs as the primary driving forces, along with an emerging new ExpressCard standard, component and system pricing will continue to fall, thus spawning even more designs. Also driving PCIe deployment is a robust interoperability effort, including frequent PCIe "plug fests" that are well attended by vendors and other workshops that help ensure the ability to mix and match components from those vendors. These efforts, combined with technological and market momentum, are helping to guide the ongoing migration from PCI/X to PCIe technology. ECD

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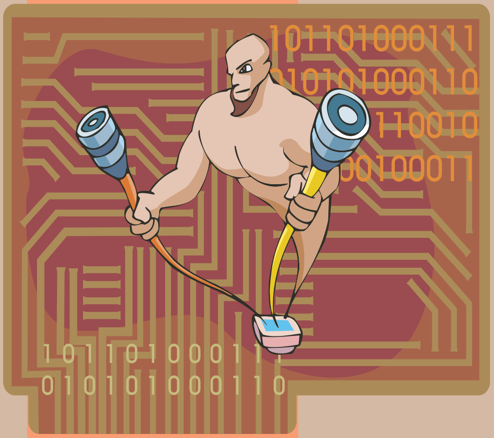
Platform ASICs provide PCI Express alternative



By Greg Martin, Grant Lindberg, and Jusak Effendy

This article looks at the options that should be considered when developing digital designs with a PCI Express interface. The choices range from cell-based ASICs, Platform ASICs, and FPGAs. Each of these has unique pros and cons. This article discusses the key considerations that should be examined before making a choice.

PCI Express is a high-speed communications standard that requires a high-performance logic implementation. Cell-based ASICs provide the highest performance and most dense solution. In certain circumstances, including mid- and low-volume applications, however, cell-based ASICs are not always the best choice, and other technologies need to be considered.

FPGAs may be suitable for some applications, especially where their lower performance and higher unit cost can be tolerated. For many mid- and low-volume applications, Platform ASICs are the best solution. High-performance Platform ASICs, such as the RapidChip Platform ASIC from LSI Logic, provide approximately 80 percent of cell-based ASIC performance and density, while shortening time to market and lowering upfront costs.

When choosing between cell-based ASICs, Platform ASICs, and FPGAs, there are obviously many factors to consider, most of these are beyond the scope of this article. When specifically targeting a PCI Express application, the most important consideration is the raw logic speed. This can have a major impact on many characteristics of the final PCI Express interface.

Gate count

If the performance of an implementation technology is not high enough, some RTL modifications need to be performed for a PCI Express core to achieve the required performance level. One of the most significant modifications is the widening of data paths, which increases the overall required gate count.

For example, consider a typical eight-lane (32 Gbps aggregate) PCI Express interface. The data paths can be implemented with 64 bits clocked at 250 MHz or with a 128 bits clocked at 125 MHz.

A cell-based ASIC implementation can easily achieve 250 MHz, allowing 64-bit data paths to be used. Likewise, when implemented in a high-performance Platform ASIC, the same core can easily achieve 250 MHz, again allowing the smaller, and more efficient 64-bit data path implementation to be used.

For an FPGA implementation, the story is very different. It is extremely difficult, if not impossible, to successfully implement any reasonably complicated digital design (with ~20 logic levels) at 250 MHz, even with the latest 90 nm FPGAs.

The example x8 PCI Express core described previously requires a 125 MHz clock with a 128-bit data path when implemented in an FPGA.

Since these data paths comprise a large portion of the entire design, this will have a major impact on the gate count. An FPGA implementation may require up to 60 percent more logic resources than the Platform ASIC or cell-based ASIC version.

Latency

The latency of a PCI Express controller greatly influences the overall performance of the interface and sometimes the entire system. The round-trip latency of a design is measured from the PIPE Tx to the PIPE Rx, going across the physical, link, and transaction layers. A PCI Express controller implemented as part of a cell-based ASIC will typically have a round-trip latency of 15 to 25 clock cycles.

If a controller has 20 clock cycles round-trip latency when implemented in a cell-based or Platform ASIC at 250 MHz, the clock cycle latency is 20 x 4 ns = 80 ns. If the same controller is implemented in an FPGA clocked at 125 MHz, the clock cycle latency doubles (20 x 8 ns = 160 ns), a 2x increase in system delay.

Link utilization

The increased latency FPGAs suffer from can also translate into degraded link utilization. For example, consider the utilization of a PCI Express egress link with a cell-based ASIC link partner. Figure 1a shows the PCI Express transmit path implemented in a Platform ASIC/cell-based ASIC. Figure 1b shows the PCI Express transmit path implemented in an FPGA.

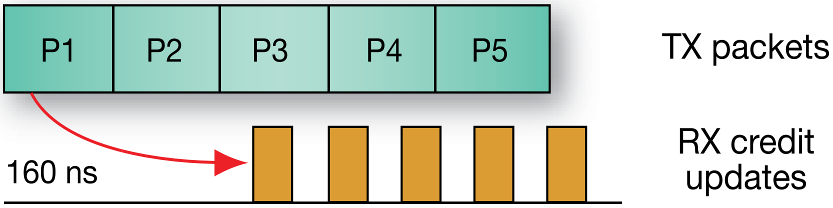


Figure 2a

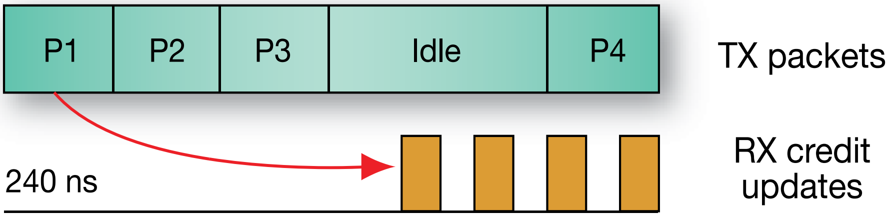


Figure 2b

In the transmit data path, the PCI Express core sends packets to the link partner buffer. When packets leave this buffer, credits are released back to the transmitting PCI Express core. The size of the receive buffer in the link partner and the latency in receiving the credit back to the transmitting PCI Express core determines the efficiency of the link.

The fixed size of the Virtual Channel (VC) buffer on the receiving cell-based ASIC link partner will typically be optimized for connection to a device with corresponding latency. Therefore, it will work most efficiently when connected to a device with corresponding latency, either a cell-based ASIC or Platform ASIC.

If the end-to-end latency involved in sending a packet from the transmitting PCI Express core and receiving the credit back is much more than the typical number assumed in the buffer size estimation, the link will start idling due to credit starvation. Credit starvation occurs when the receiving buffer is not large enough to handle higher than predicted end-to-end latency.

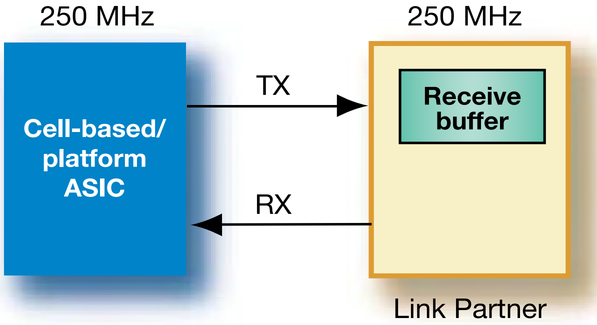


Figure 1a

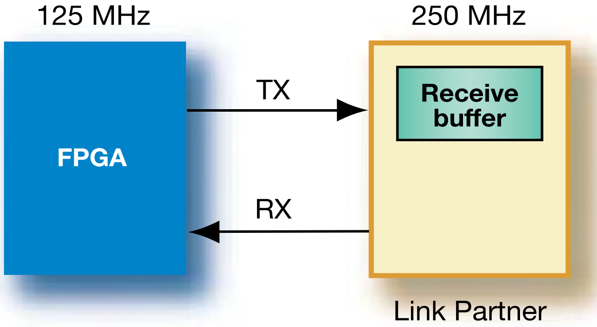


Figure 1b

A simple comparison between a Platform ASIC and FPGA implementation is shown in Figures 2a and 2b. The analysis is simplified by excluding such effects as packet size and credit release policy, and so on. Figure 2a shows how a Platform ASIC and cell-based ASIC implementation continuously sends packets. The low latency allows credits to be received back fast enough to avoid starvation. In contrast, Figure 2b shows how the higher latency with an FPGA implementation causes a longer delay for credit updates to occur, causing the link to go idle.

This example only considers the case of posted-write packet types, although the effects also apply to other packet types and multi-VC cases.

A major component of the credit latency path is internal to the controller. Let's assume the round-trip latency inside the link partner is 20 cycles (at 250 MHz). The most significant portion of the end-to-end credit return delay is the sum of the round-trip latencies of both controllers, that is, 20 x 4 ns for the link partner plus 20 x 4 ns for the Platform ASIC/cell-based ASIC PCI Express transmit core. This gives a total credit return latency of 160 ns.

With an FPGA implementation of the PCI Express transmit core, the calculation is 20 x 4 ns for the link partner plus 20 x 8 ns for the FPGA, giving a total of 240 ns. If the buffer in the link partner was designed for a system with 160 ns credit return delay, then the link utilization for the FPGA implementation will be reduced by 33 percent.

Buffer size

The receive path to a PCI Express core also has similar link utilization considerations. In an FPGA implementation, the receive VC buffer size must be increased by 50 percent to absorb the increase in end-to-end latency (240 ns instead of 160 ns, for the previous example). If the receive buffer is not increased, the receive data path will also suffer from reduced link utilization.

Overall performance

In addition to the local credit starvation and link utilization issues, the increased latency of an FPGA implementation affects other areas of system performance. Figures 3a and 3b highlight how latency affects the read performance in a system.

For a given number of outstanding reads from a node, any increased latency in receiving a response adds significant waiting time for the read initiator. This reduces overall read bandwidth. If the read data contains assembly code to be executed or data packets to be processed, then the impact of the additional read delay may be even greater.

> Platform ASICs such as the RapidChip Platform ASIC from LSI Logic, with significantly reduced up-front costs, are able to achieve performance close to that of a cell-based ASIC, making them ideal for mid-volume PCI Express applications.

Summary

When deciding on a PCI Express solution, it is important to weigh the pros and cons of the underlying implementation technology employed. Both cell-based ASICs and Platform ASICs provide an excellent base on which to build a solid, reliable PCI Express design.

Platform ASICs such as the RapidChip Platform ASIC from LSI Logic, with significantly reduced up-front costs, are able to achieve performance close to that of a cell-based ASIC, making them ideal for mid-volume PCI Express applications. FPGAs, on the other hand, suffer from increased latency, degraded link utilization, and increased silicon cost when used to implement a PCI Express controller. ECD

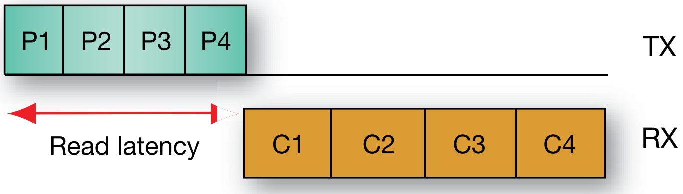


Figure 3a

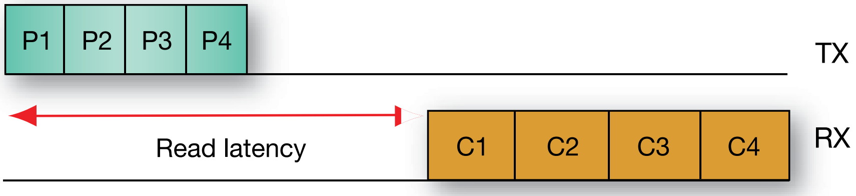


Figure 3b

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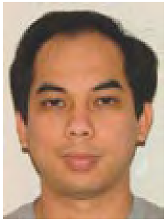

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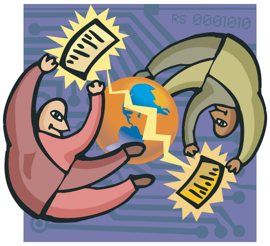

Wanted: Higher bandwidth, greater flexibility

By Robert Hollingsworth

PCI Express is now entering mainstream applications. It is common on today's desktop and servers, and high-end, high-performance devices and applications are quickly embracing its performance advantages. However, the high-volume consumer markets cannot take advantage of it just yet. What is the snag that is keeping PCI Express devices from widespread implementation in the mass markets? This article will take a look at the current state of affairs and make predictions about when PCI Express devices can expect to become ubiquitous.

PCI Express: Not just fast, but small and simple, too

As a shift takes place in system architectures from parallel to serial communications and fast-paced innovations occur in computing and communications, an increasing need for interconnects to facilitate higher bandwidth and greater system flexibility in smaller package solutions arises. Many industry observers believe that speed will drive the widespread implementation of PCI Express (PCIe), a new industry standard for high-performance I/O interconnects. PCIe is very fast – so fast that companies such as Intel, Broadcom, and Marvel are already incorporating it into their gigabyte Ethernet controllers, while ATI and Nvidia are implementing PCIe in their high-speed graphics adapters. Other real advantages to PCIe are its low pin count, flexible software interface, and point-to-point architecture. However, the biggest obstacle to widespread adoption of PCIe across all types of markets is the current high cost of the silicon needed to implement the interface.

The big picture

One key to the mass implementation of PCIe will be the narrow bus that will enable fast throughput and lower latency. Wider buses consume a larger number of pins. The number of pins required, as systems become increasingly feature rich, has also become a major limiting factor in optimizing computing and communications applications. PCIe-enabled chipsets, by design, are lower in pin count, and, therefore, take up less space on the motherboard than their predecessors. Though designers of graphics and gigabyte Ethernet controllers will initially utilize PCIe, as 0.18 µm wafers become more cost effective, PCIe will become a very attractive solution for designers seeking to create lower pin count interfaces for more diverse applications.

Declining market ASPs have made it important to drive cost efficiencies, which will also help drive the acceptance of lower pin solutions such as PCIe. The PCIe interface allows for great variation in the number of pins used in an application and can provide excellent throughput using only five pins of real estate. Because of the high speeds achieved by PCIe (up to 2.5 gigabytes per second or GBps), an implementation that uses only five of the 40 pins available would still provide 2.5 gigabits per second (Gbps) throughput. The standard PCI interface requires at least 56 pins and is still 10 times slower than five pin solutions at PCIe speed. Product designers will appreciate the flexibility to incorporate only as many pins as needed to achieve the required transfer speeds. The ability of PCIe to support new topologies, or board configurations, in addition to working with the current PCI-infrastructure, also allows system designers greater flexibility in placing their system resources. Product designers and manufacturers in a broad range of non-PC niche markets will take advantage of the flexibility of unrestricted driver software to integrate this technology into unique products. Connectivity applications outside the PC that will benefit include consumer products such as digital multimedia applications and other embedded networking communications.

It's not just for PCs any more

Although PCIe has been touted as a means to enhance the performance of PC workstations and graphics controllers, those who are lauding PCIe primarily for its speed and utility in the PC market are overlooking a very important point. PCIe parallels USB 2.0 in terms of usability and performance – both are fast, hot pluggable, and capable of multispeed implementations. The differentiation between PCIe and USB 2.0, and PCIe's standout feature, exists in its programming interface. Because PCIe requires no class drivers, it is destined to be the interconnect of choice for product markets unsupported by Microsoft. The greatest benefits of PCIe will no doubt be realized in these niche markets, where it will provide a means to achieve greater speed with fewer pins for tighter board designs, while using an unrestricted driver interface, ultimately at lower costs.

Certainly, for graphics controllers, PCIe can provide faster transfer rates, increased bandwidth, and scalability, and offer the

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ability to support faster memory and serial connections, while older AGP graphic interfaces have inherent limitations with their common clock. But class-driver independence positions PCIe for use in a host of nonstandard PC applications. PCIe will also be a welcome interface to manufacturers of TV tuners, DVD applications, set-top boxes, printers, telephone line card interfaces, and so on, all of which currently use wide buses such as PCI or proprietary local processor buses and are on an interminable quest to streamline their hardware real estate in a high-performance yet cost-efficient manner. It is the PCIe driver-friendly interface that will make all this feasible.

Another factor in the acceptance of PCIe in non-PC solutions is the point-to-point nature of its architecture. By avoiding the technical challenges associated with a multipoint bus design like PCI, issues such as bus loading, interrupt latency, and configuration complexity are significantly reduced. Even though implementing system designs using 2.5 GHz communications channels is not trivial, eliminating the complications of a shared bus enables successive generations of designs to better leverage successful implementations.

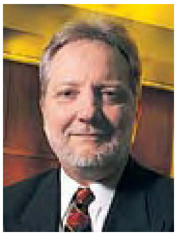
So where's the snag?

Ironically, although PCIe ultimately will provide an economical means to improve interconnectivity significantly, the real obstacle to the adoption of PCIe across all types of markets can be expressed in five words: the high cost of silicon. The largest geometry recommended for PCIe is 0.18 µm. The fact is that the industry experienced a capacity crunch in 2003, and still, silicon prices are not dropping as precipitously as we might have hoped. It could still be some time before silicon prices drop enough so that PCIe's manufacture and implementation costs would be low enough to become cost effective for products with tight profit margins.

Gigabyte Ethernet and high-speed graphics adapters have the performance requirements and associated price points that can absorb the high cost of the silicon required to produce PCIe interfaces, but this is not so with many other products. Unfortunately, the current cost of silicon and its consequential price push for PCIe manufacture makes PCIe prohibitively expensive for the more cost-protected implementations that it will one day dominate. That day, however, is probably two years away.

Adding it up

The bottom line is that PCIe has great speed going for it, but it's the pin-count flexibility and ease-of-driver implementation that will fuel future growth for the PCIe market, and that market may be tremendous. **ECD**



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New intelligent multithread processors benefit from integrated and innovative tools for code debug, programming, and test

By Bob Burrill

A new wave of intelligent, multithread processors is becoming available to design engineers. The new processors feature multicore, multithread processing to enable throughput many times faster than traditional single-thread processors. With these new complex processors, a set of JTAG debugging, programming, and test tools is filling the need to provide fast and easy integration of the new processors into the products that will feed the new network-centric infrastructure.

With the increasing need to move processing outside the confines of a single box to an interconnected world of devices, today's single-thread processor architecture is showing its performance limitations. At every point in the new networked infrastructure lie devices in need of new services, improved bandwidth, deeper content inspection, complete data security, and accelerated applications.

This new packet-oriented environment is characterized by high memory access latencies, which are not effectively managed by conventional processor architectures. In this case, single-thread processing will severely impact processor performance and workload efficiency when memory accesses aren't immediately serviced and packets back up in the queue, sending conventional processors into a stall and wasting valuable processing cycles.

The new wave of intelligent, multithread processors are system-on-chip processors that combine the functions of several ASICs, network processing units, and coprocessors to reduce hardware and software costs and complexity. The multicore, multithread processing capability of these processors enables throughput many times faster than traditional single-thread processors.

The need for a new generation of processors

The fundamental difference between core speeds and memory or I/O latencies means that today's processor architectures cannot deliver meaningful performance for connected computing. These processors are usually waiting for data. The need for data security significantly contributes to these delays (stalls) as well, as the processor must not only move the data, but also run security application code at the same time. These stalls can occur as much as 90 percent of the time that the processor is active.

Until now, processor designs attempted to overcome these barriers by using deeper pipelines, superscalar (multi-issue) operations, and larger caches. However, those efforts are yielding diminishing returns because the data processing in network applications occurs at the macro or packet level, not at the instruction level.

Next-generation processors, such as the Raza Microelectronics (RMI) XLR processor family, overcome these issues by integrating a set of enhanced MIPS64-based cores into a single processor chip. Each core includes four hardware threads, integrating up to 32 threads or virtual CPUs in eight identical processor cores. Unlike single-threaded, multi-issue designs, this architecture is well suited to today's increasingly network-oriented computing environment and can significantly reduce stalls. Using up to 32 virtual processors enables deep inspection of multiple packets at once, fast decisions on routing within the chip, and quick passing of the processed packets on their way, in their proper order.

Applications of the processors include integrated security (firewall, VPN, anti-virus, intrusion detection and prevention), Web services, virtualized storage, load balancing, server offload, and intelligent routing and switching, in which content awareness and application intelligence are becoming more important to increasing enterprise productivity.

There are a variety of ways to use the threads of the new processor to increase execution efficiency and accommodate the specific needs of networking-centric applications. In this environment, when one hardware thread is waiting on a memory request, the next thread in the core can immediately begin processing additional data, mitigating latencies, and dramatically improving overall throughput. The threads also can be used in multiple combinations and to replace typical discrete coprocessor functions. And in more compute-intensive applications, a single core can be programmed to dedicate all processing resources and available clock cycles to a single, focused task.

A single-core, single-thread approach runs all tasks in a serial fashion. New processing cannot begin until the previous process is complete. This results in significant memory latency delay accumulation as shown in Figure 1, courtesy of RMI.

The multithread approach takes advantage of, and more fully exploits, the packet-level parallelism commonly found in today's converged computing and networking applications. This workload efficiency improvement is shown in Figure 1. Note in this four-way threaded example, a packet is operated on every fourth cycle. In the clock cycle immediately following that used for packet 1 (yellow), thread 2 can begin operating on packet 2 (blue). Likewise, thread 3 (green) can immediately follow thread 2, and thread 4 (red) can immediately follow thread 3. The process continues among the four separate threads and corresponding packets. The benefit becomes most apparent in the event of a cache miss, during which time the processor can apply useful work to other independent packets while other threads wait for memory. The memory latencies are effectively mitigated and the workload efficiency is highly optimized.

Development tools to support multicore and multithread features

Multiple cores and multiple threads in the chip, and combining multiple functions into a single chip design, make for a very powerful and cost-effective processor. However, the chips also bring a whole new level of complexity to product design, debugging, programming, and test.

To overcome that complexity, implementing the new technology into designers' products, a key element of introducing new chips, must be made easier. Code debugging, programming, and test must be considered early in the cycle of new chip design. This part

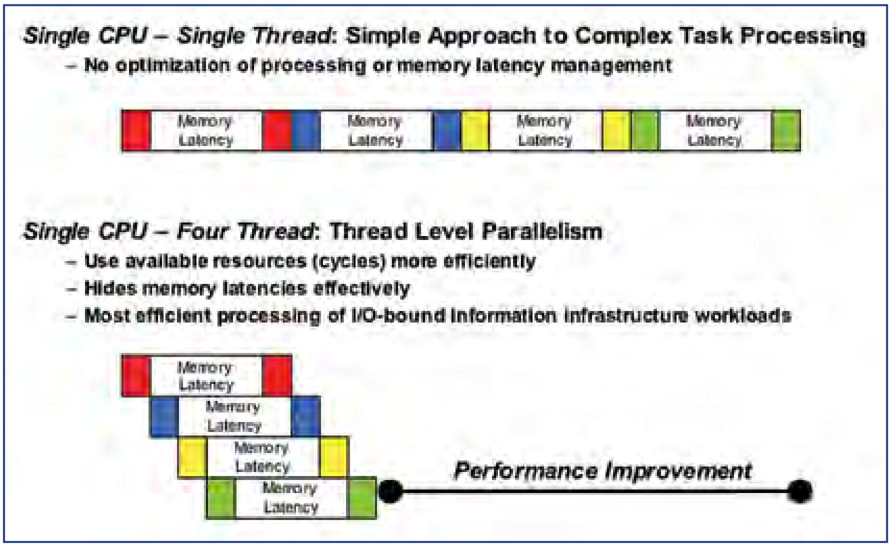
Single CPU – Single Thread: Simple Approach to Complex Task Processing
– No optimization of processing or memory latency management
Memory Latency
Memory Latency
Memory Latency
Memory Latency
Single CPU – Four Thread: Thread Level Parallelism
– Use available resources (cycles) more efficiently
– Hides memory latencies effectively
– Most efficient processing of I/O-bound information infrastructure workloads
Memory Latency
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Figure 1

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of chip development is especially important with the proliferation in the number of available chipsets. Chipmakers need to have tools ready and available to support development when people jump on the bandwagon of a new chipset and production volumes explode.

Debugging multicore, multithread processors

The design engineer faces a new challenge when implementing multicore, multithread chips – to separate and track all of the simultaneous processing occurring in the processor. The JTAG emulator software provided by Corelis for the XLR gives engineers source-level debugging for multiple processors that partitions the individual processor hardware and software resources into a multiwindowed environment. Each thread appears as a separate (virtual) CPU. Engineers can view and modify registers and memory, set software breakpoints, and step through code for every thread and every core independent of the other threads and cores. The XLR processor has an eight-bank Level-2 cache that can process up to eight simultaneous requests from any of the cores and provide a separate hardware instruction and hardware data breakpoint for each of the threads.

Seeing each thread separately, as depicted in Figure 2, provides a view into the multiple ways these processors operate on each packet. For example, threads can request security operations using a new high-speed communications ring architecture within the chip. The engineer can monitor this dedicated security thread at the same time as other processing functions to verify that information will remain secure and identify any packets out of sequence.

The Corelis emulator paired with the XLR processor offers an extensive macro and scripting capability, and can interpret command files written in a structured *C-like* language, providing an excellent tool for board bring-up, driver and firmware development, and software application debugging of these new processors.

The benefits of quicker development cycles, faster time to market, and flexibility in reacting to the market in terms of new features or technology trends, is obvious. By partitioning the code so that each task is treated as a separate virtual CPU, design engineers can isolate and redesign the code for only the virtual CPU that will handle that new feature or process. In viewing a separate CPU, the engineer gains a significant performance improvement in debugging source code over the traditional method of using thread-dependent breakpoints and kernel-awareness modules.

Continuing tool development

JTAG emulator functions can be expanded into boundary-scan testing and programming by using the same JTAG controller that the emulator is using (saving on hardware) and adding additional software for boundary-scan testing and in-system programming such as the Corelis ScanExpress family of boundary-scan test tools.

Tracking the sometimes simultaneous transactions on the unique communication rings within each XLR chip poses another challenge. These are extremely high-speed (processor core clock frequency) communication rings providing pointers to the packet data as it is sent between processors, I/O, and so on. A boundary-scan chain cannot track these transactions at the 1.5 GHz processor clock speed. Solving this problem involves implementing an internal trace in the silicon and accessing it with the JTAG interface, which has seen similar successful implementations for chips developed by several CPU vendors.

Summary

Multicore, multithread intelligent networking processors can provide a key to enable the next generation of information infrastructure devices. The development environment around these chips has moved up to a new level of complexity, but the reasons for using the new architecture are so compelling that multithread processors are sure to grow quickly in application. Fortunately, a new set of debugging, programming, and testing tools closely integrated with the architecture are evolving right alongside these chips. The combination is enabling the flexibility to feed a fast-changing market and shorter development cycles for product designers and manufacturers. **ECD**

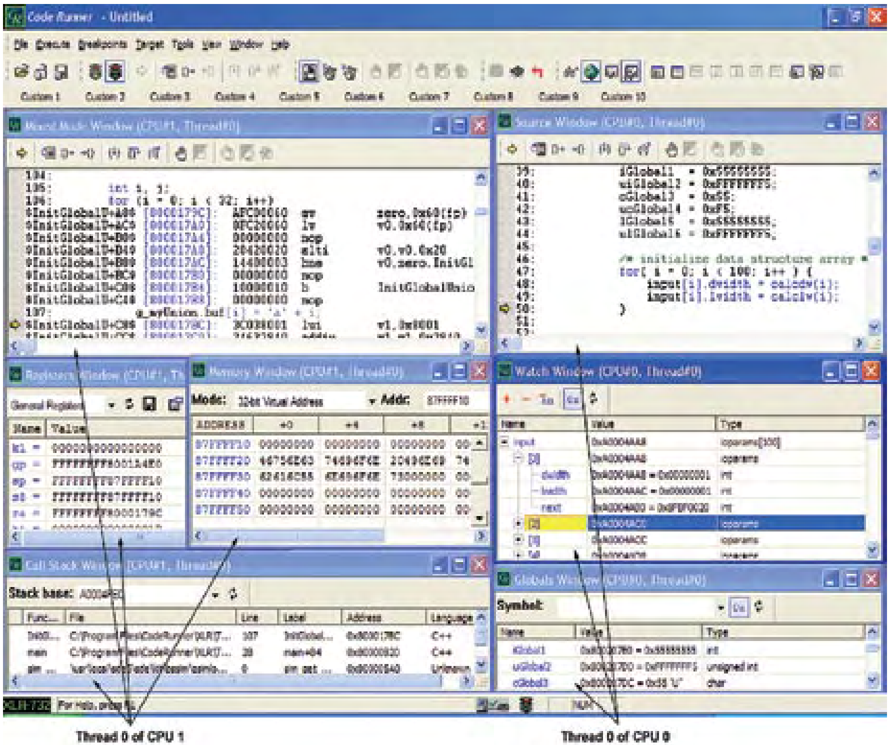
Code Runner - Untitled
Mixed Mode Window (CPU#1, Thread#0)
Source Window (CPU#0, Thread#0)
Registers Window (CPU#1, Th
Memory Window (CPU#1, Thread#0)
Watch Window (CPU#0, Thread#0)
Call Stack Window (CPU#1, Thread#0)
Globals Window (CPU#0, Thread#0)
Thread 0 of CPU 1
Thread 0 of CPU 0

Figure 2

__Bob Burrill__ is CodeRunner product manager at Corelis, Inc., with more than 30 years of experience in the hardware, software, and system design of embedded systems. Five years ago, he moved into the development of software development tools after having used a variety of them for many years. Bob has a BSEE from the University of Washington and an MSE from Arizona State University.

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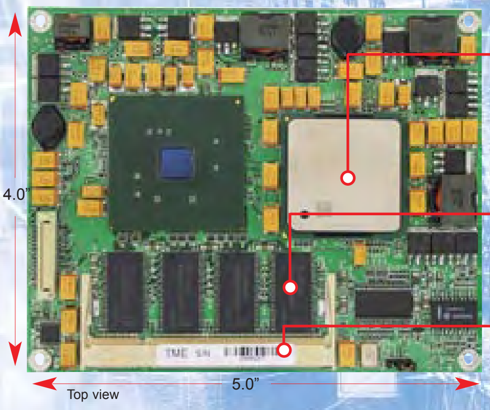

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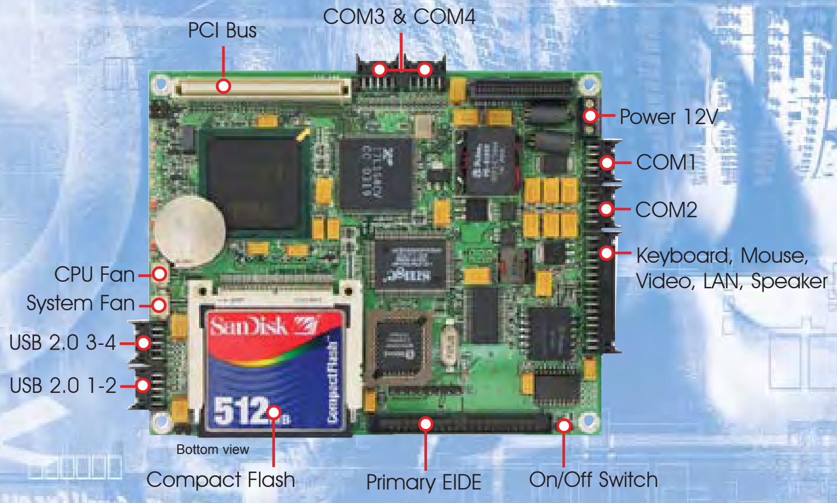

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PCI Express enhances computer module abilities

By Jerry Gipper

PCI Express (PCIe) is significantly affecting computer modules. Many of the benefits of PCI Express play well into the overall goals of computer modules. Besides the obvious benefits of scalable architecture, high bandwidth, and software compatibility with PCI bus, PCI Express offers many other advantages critical to computer module designs.

- **Hot swappable –** Modules may be removed under power. The serial bus fabrics and transfer protocols allow removing and replacing of modules without exceptional design considerations. Many computer modules are designed to add functionality to a computer as needed, so the ability to hot swap is a major consideration. PCI Express gives developers an integrated hot-plug feature for the same cost as non-hot-pluggable options, as well as closed chassis, tool-less adapter installation and removal, which significantly reduces system downtime.
- **Low power consumption –** The serial bus of PCI Express uses much less power for signal switching than typical parallel buses. The power budgets of many computer modules, especially the smaller form factors, are very restricted. Low power consumption is a plus. Advanced power-management features of PCI Express are expected to be used aggressively.
- **Higher wattage –** More pins can be dedicated to power for modules that have a need and the ability to dissipate higher wattages. Combined with the inherent low power consumption of the interface, the power window is much larger for designers.
- **Quality of service policies –** Modules can be designed to be more reliable and robust to better handle data processing and transfers through modules.
- **Peer-to-peer communication via switches –** Fabric switch architectures give designers more options for how they structure an embedded computer system. Performance can be optimized to meet the application needs by setting up the appropriate peer-to-peer communication topology such as rings, stars, or meshes.
- **Possibility of multiple linked modules –** Certain applications, such as graphics or signal processing, work best in a multiple link stage structure. PCI Express makes this possible.
- **Integration into processors and chipsets –** Though not a benefit of PCI Express itself, the fact that PCI Express is being widely adopted by all the semiconductor suppliers means that processors and chipsets will be native PCI Express-enabled. This simplifies module design, lowers cost, and lowers board space requirements. Computer modules can follow the electronics tradition of more functionality/performance for less cost.

All of these benefits of PCI Express greatly enhance the capability of computer modules. The PCI-SIG has established at least three computer module specifications:

- **PCI Express Card Electromechanical Specification**
  - Addresses add-in cards for ATX-based desktop applications
- **PCI Express Mini Card Electromechanical Specification** (see Figure 1)
  - Addresses small card form factor for mobile and communications systems. Figure 1 shows ExpressCard/34 and ExpressCard/54 module components and card kits from FCI.
- **PCI Express ExpressModule Electromechanical Specification**
  - Latest addition defines removable modular I/O adapters for closed chassis servers and workstations

The PCI-SIG is also working on a PCI Express Wireless Form Factor.

We are seeing all of the viable and established computer module and mezzanine form factors adopt PCI Express as the next-generation or switch-fabric alternative to their specifications. The benefits of PCI Express simplify and greatly enhance the abilities of these established form factors.

Table 1 (on page 38) lists many of the established form factors that are adopting PCI Express along with their intended usage.

Copies of these specifications are available from the developing organization. Many other existing form factors may be updated to reflect a PCI Express variation. You can also expect that many other implementations of PCI Express will be introduced as it becomes more ubiquitous in the industry.

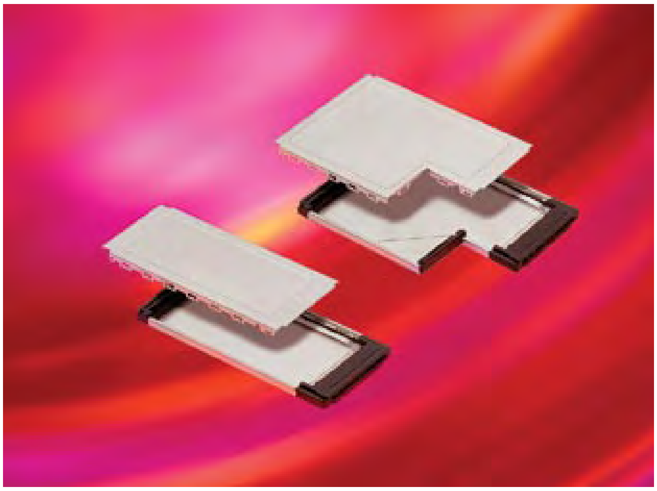

Figure 1

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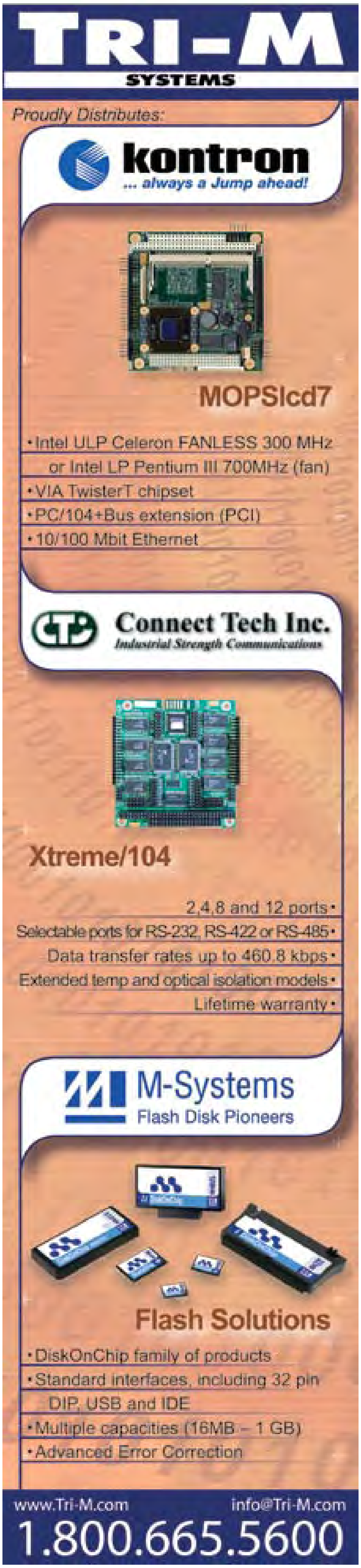

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PCI Express is a revolutionary hardware change. Despite the fact that many form factors remain similar, a change in connector technology or layout is usually required to support the high speeds of PCI Express. These new connectors necessitate new motherboards or backplanes for the embedded system. The software model is essentially the same as the PCI bus model, so the software side of the equation sees this as an evolutionary change. The impact on software models is substantially less than on the hardware.

Unfortunately, the revolutionary nature of the hardware change allows developers to consider system-level changes. Suppliers have tried to make the change as minimal as possible, but there is no avoiding the fact that parallel buses and serial buses are different. New options exist today that were not available a few years ago when system architecture choices were made. Be sure to study all of the existing options and select the options that will give you the best return on investment. The good news is that serial buses appear to have a long life-cycle run ahead. You may change between serial fabrics, but the basic mechanical structure looks viable for the long term.

More good news is that PCI Express opens the doors to many new applications that were not possible with parallel buses or lower bandwidth serial buses. The creative nature of the embedded computer design community is sure to find many exciting applications of PCI Express technology that will make life better for all of us.

Companies are just starting to make product announcements for PCI Express-enabled modules. PCI Express is mainstream in desktop computers now. You can expect much activity in this area during the coming months.

PCI Express-enabled modules

Module	Developing organization	Intended usage	Website
PCIe Card	PCI-SIG	Add-in cards for ATX-based desktop applications.	www.pcisig.com
PCIe Mini Card (CEM)	PCI-SIG	Small card form factor for mobile and communications systems, replaces PCMCIA/Card bus-type cards.	www.pcisig.com
PCIe ExpressModule	PCI-SIG	Removable modular I/O adapters for closed chassis servers and workstations.	www.pcisig.com
EPIC Express	EPIC Express	Embedded Platform for Industrial Computing (EPIC) Express stackable modules based on PC/104 form factor. Includes base and modules.	www.epic-express.org
AdvancedMC	PICMG	Hot pluggable mezzanine card for use on blades with low profile restrictions.	www.picmg.com
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CompactPCI Express	PICMG	3U/6U multipurpose blade. Update of CompactPCI to enable use of PCIe.	www.picmg.com
PXI Express	PXI Systems Alliance	PXI-enabled CompactPCI Express blade for test and measurement applications.	www.pxisa.org
XMC	VITA	Based on the Common Mezzanine Card (CMC) and PCI Mezzanine Card (PMC) for use on blades with low profile restrictions.	www.vita.com
VPX	VITA	3U/6U multipurpose blade. Primarily targeted at applications in a rugged environment.	www.vita.com
VXS	VITA	Upgrade to VMEbus to enable PCIe on P0.	www.vita.com

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M457					•							
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MFCC 8443								•				
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EP425M											•	
EP82xxM					•							
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esd												**www.esd-electronics.com**
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XPedite1000	•											
XPedite1001	•											
XPedite1005	•											
XPedite4000								•				
XPedite5000						•						
XPedite6200				•								
XPort1000					•							
XPort1002					•							
XPort2001					•							
XPort2100						•						
GE Fanuc Automation												**www.gefanuc.com/embedded**
PMC721TX							•					
Interface Concept												**www.interfaceconcept.com**
IC-e6-PMCa				•								
IC-PQ2-PMCa					•							
IC-PQ2-PMCb					•							

	AMCC	AMD	Analog Devices	Freescale			IBM		Intel			TI
Company/Model Number	PowerPC 4xx	SC2200 GEODE	SHARC	MPC74xx	MPC82xx	MPC85xx	PowerPC 4xx	PowerPC 7xx	Pentium III	Pentium M	Xscale IXP425	TMS320C64
Interface Concept (continued)												www.interfaceconcept.com
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Spectrum Signal Processing												www.spectrumsignal.com
ePMC-8310												•
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Technobox												www.technobox.com
3797		•										
Varisys Ltd												www.varisys.co.uk
VM145				•								
VMETRO												www.vmetro.com
TS-C43			•									

New PRODUCTS

By Chad Lumsden

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AVIONICS

SEAKR Engineering, Inc.

Website: www.seakr.com
Model: RCC-R **RSC No:** 23623
Space-based reconfigurable computer (dual Xilinx FPGAs) • High speed memory 512 MB DDR2 SDRAM • 6U CompactPCI • High speed RapidIO (serial and parallel) • Radiation Tolerance (TID 30KRAD)

BACKPLANE

SMA Computers

Website: www.SMAcomputers.com
Model: Backplanes **RSC No:** 23108
3U CompactPCI backplanes • Available with one to eight slots • Over eight slots with bridging • Power backplanes • Rear I/O options

BACKPLANE: HOT SWAP COMPLIANT

Schroff

Website: www.schroff.us
Model: Backplanes **RSC No:** 23109
A series of CompactPCI backplanes with bridging capability • Rear I/O on both 6U and 3U versions • PICMG 2.0 R3-compliant • Hot-swap capability • Available with two to eight slots • May be mounted side-by-side without the loss of any slots, using the flat Schroff-bridge located under the rear I/O boards • By using 4- or 7-slot extension backplanes. a 19" chassis can accommodate as many as 21 slots • Backplanes and Schroff-bridge operate at up to 66 MHz • High-capacity ceramic capacitors provide safe decoupling of high-frequency surge voltages • Operating temperature is -30 °C to 70 °C • Voltage supply is available with a screw terminal, M connector, or ATX connector

CHIPS & CORES: IP

VMETRO

Website: www.vmetro.com
Model: Serial FPDP IP Core **RSC No:** 23649
Provides support for all the mandatory and optional features of the serial FPDP specification, bringing the power of this serial interface to any Xilinx Virtex-II Pro FPGA with available RocketIO interfaces • The IP core supports all three signaling rates (1.0625 Gbps, 2.125 Gbps, and 2.5 Gbps) and at the highest link speed provides reliable, sustained data transfer bandwidths of 247 MBps • 32-bit data + 4-bit control/status back end interface to client application • Complete ANSI/VITA 17.1-2003 implementation allows links to support any Serial FPDP mode • Compatible with VMETRO's PMC-FPGA03/F and VPF1

CHIPS & CORES: MIPS

AccelChip Inc.

Website: www.accelchip.com
Model: IP-Explorer **RSC No:** 23657
MATLAB-based algorithmic synthesis generates technology-optimized RTL • Automated floating- to fixed-point conversion • IP-Explorer technology enables heuristic-driven selection of hardware architecture at algorithmic level • Complete automated verification flow with automatic testbench generation • Hardware optimizations including loop rolling/unrolling, matrix multiplication expansion, RAM/ROM memory mapping, pipeline insertion, and shift register mapping • Model generators for Simulink and Xilinx System Generator for DSP

DATA ACQUISITION

EuroTecH SpA

Website: www.eurotech.it
Model: DAQ-1276 PC/104 24+24 **RSC No:** 23633
48-channel galvanically isolated digital I/O: 24 inputs (+5 V to +24 V nominal range), 24 outputs (+5 V to +30 V switching range) • Two high-power MOSFET outputs • Three counter/timers available (8254) software selectable counter configuration, 8 MHz clock • I/O pin functions freely programmable • Input masking and complex interrupt modes, counters up to 16 bits, up to 8 incremental encoder channels, PWM outputs and stepper motor drive, custom functions upon request • FlexiSet software configurable nonvolatile BASE address and IRQ configuration, IRQ sharing supported • FPGA programmable through ISA bus, in-circuit firmware upgrading

Model: DAQ-1277 PC/104 24+24 **RSC No:** 23634
48-channel multifunction digital I/O • Three counter/timers available (8254) with software selectable counter configuration, 8 MHz clock • I/O pin functions freely programmable • Input masking, complex interrupt modes, counters up to 16 bits, up to 8 incremental encoder channels, PWM outputs, custom functions upon request • FlexiSet software configurable nonvolatile BASE address and IRQ configuration, IRQ sharing supported • FPGA programmable through ISA bus, in-circuit firmware upgrading • Software configurable bit programmable direction and bit programmable pull-up/down on all lines

Sundance Multiprocessor Technology Ltd.

Website: www.sundance.com
Model: SMT390 **RSC No:** 23552
2 x 12 bit A/Ds @ 210 MHz • 2 x 4 channels rocket serial links, 400 MBps data bus, 20 MBps comports • Virtex II Pro FPGA for custom designs

DATACOM: ETHERNET

Technologic Systems

Website: www.embeddedARM.com
Model: Ethernet Adaptor (TS-ETH10) **RSC No:** 23572
10 MB Ethernet • LEDS for Ethernet link and activity • Four separate address decodes enable stacking up to four high

DATACOM: SERIAL CONTROLLER

TEWS Technologies LLC

Website: www.tews.com
Model: TPMC462 **RSC No:** 23557
4 channel serial interface RS-232/422 • Standard single-width 32-bit PMC module conforming to IEEE P1386.1 • Quad UART: Exar XR17D154 • Support of RxD, TxD, RTS, CTS, and GND for each RS-232 channel; RxD+/-, TxD+/-, and GND for each RS-422 channel • One channel offers extended support (full modem or RTS+/- and CTS+/-) • Programmable baud rates: RS-232: up to 921.6 kbps RS-422: up to 5.5296 MBps • 64-byte transmit FIFO per channel • 64-byte receive FIFO per channel • Readable FIFO levels • General purpose 16-bit timer/counter • ESD protected transceiver (up to ± 15 kV) • Operating temperature -40 °C to +85 °C

ENCLOSURE + CARD RACK + POWER SUPPLY

Technologic Systems

Website: www.embeddedARM.com
Model: TS-7200, TS-7250 **RSC No:** 23591
Supports TS-7200 & TS-7250 • 8-38 VDC input provides +5 VDC, surge suppression on power input • COM ports adapted to nine-pin Sub-D • Power good LED visible • Status LEDs for Ethernet visible • Extra DB9 allows third COM port, eight DIO signals, or eight A/D inputs

PRODUCTS NEW PRODUCTS

INDUSTRIAL COMPUTERS

Small PC Computers

Website: www.smallpc.com
Model: SC200 **RSC No:** 23686

P3 or PM CPU in small, rugged package (10.6" x 2.4" x 6.4") • Panel or DIN rail mounting • PC/104 expansion • DC power 8-28 V • Optional solid-state flash drive • Optional extended temperature -40 °C to +75 °C • Windows XP/2000/XP Embedded, Red Hat Linux

MEZZANINE: CCPMC

Radstone Embedded Computing

Website: www.radstone.com
Model: ICS-8554 **RSC No:** 23626

Four ADC channels: 14 bits @ 80 MHz • Two GrayChip 4016 DDC ASICs • 3M gate Xilinx Virtex II FPGA • 2 MB of FIFO storage • Pn4 user I/O supports LVTTL or LVDS signaling levels • Windows, Linux, and VxWorks device drivers • Extensive application and technical support available

Model: ICS-8552 **RSC No:** 23627

Two ADC channels (Texas Instruments ADS5424): 14 bits @ 105 MHz • Two GrayChip 4016 DDC ASICs • 3M gate Xilinx Virtex II FPGA • 1 PPM Temperature Compensated Crystal Oscillator (TCXO) on board • Pn4 user I/O supports LVTTL or LVDS signaling levels • Windows, Linux, and VxWorks device drivers • Extensive application and technical support available

MEZZANINE: PC•MIP

Mercury Computer Systems, Inc.

Website: www.mc.com
Model: TBA-100: ATCA Quad PMC **RSC No:** 23652

Single Pentium M 760 at 2 GHz and 533 MHz FSB • Up to 2 GB of DDR2 PC2100 SDRAM with ECC • E7520 Memory Controller with PCI Express • 6300ESB I/O controller hub • Two 2.5" Serial ATA drives onboard • Single slot PICMG 3.0 node board, 3.0 hub, or 3.1 node board • Onboard 24-port Gigabit Ethernet managed switch • Four 32/64-bit 33/66/100 MHz PCI/PCI-X PMC sites • Multiple additional I/O features and options

MOTION CONTROL

TEWS Technologies LLC

Website: www.tews.com
Model: TPMC150 **RSC No:** 23566

One to four channel synchro/resolver-to-digital converter • Standard single-width 32-bit PMC module conforming to IEEE P1386.1 • One to four channel tracking synchro/resolver-to-digital-converter • Based on DCC's RDC19230 • Signal conditioning adapter for matching wide array of synchros, resolvers • 32-bit up/down encoder counter with preload and output register per channel • 1 digital 24 V input per channel • All I/O on HD68 female connector; No P14 I/O • Operating temperature -40 °C to +85 °C

POWER SUPPLY

Technologic Systems

Website: www.embeddedARM.com
Model: Power Module (TS-12W) **RSC No:** 23571

Regulated 5 VDC via PC/104 bus • Supplies 2.4 amps • Input: 10-40 VDC input reverse polarity protection • TTL input allows remote shutdown of +5 VDC power

PROCESSOR: OTHER

Wordsworth Technology

Website: www.wordsworth.co.uk
Model: PM-1045 **RSC No:** 23549

PC/104 SiS552 CPU board with onboard DRAM, LCD/CRT VGA, LAN and audio • Embedded SiS 552 x86 MMX compatible CPU • System memory:

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Onboard 64/128 MB PC133 SDRAM • Display: SiS552 embedded with hardware 2D/video/graphics accelerators, AGP 4X compliant/fully DirectX 8 compliant • Supports shared system memory up to 128 MB • Resolution supports upto 1920 x1440 true colors, 18-bit TTL for LCD display • SSD: 1 x Disk-on-Chip socket • Audio: AC'97 CODEC • Ethernet: 1 x 10/100 Mbps RTL8100BL LAN controllers • I/O: 1 x RS-232 serial port, 1 x RS-232/422/485 serial ports, 1 x PS/2 connector for keyboard/mouse, 1 x LPT parallel port supports SPP/ECP/EPP mode, 2 x USB 1.1, 2 x IDE ATA-100, 1 x floppy • WDT: Software programmable supports 1 ~ 255 sec system reset • Digital I/O: TTL Level, 4 x inputs & 4 x outputs • Power source: Single +5 V only • Operation temperature: 0~60 °C, relative humidity: 5~95%, noncondensing

PROCESSOR: PENTIUM D

ITOX Inc.

Website: www.itox.com
Model: G7L630-B ATX **RSC No:** 23528

G7L630-B ATX and G7L330-B microATX motherboards utilize the Intel 945G Express chipset supported under Intel's Embedded Architecture program, and accept a wide performance range of Intel LGA775 packaged processors • Includes the Intel Pentium D Processor featuring dual-core architecture, Intel Pentium 4 processor supporting Hyper-Threading Technology, Intel Celeron D processor, and Intel Celeron processor • The G7L630-B ATX form factor (12" x 9.6") motherboard includes: 1-Gigabit LAN Port, 1-Serial COM Port, 8-USB 2.0 ports, Onboard 18-bit AC'97 Audio (Realtek ALC202A), Onboard Intel GMA950 Graphics, 4-Serial ATA Interfaces, 1-Ultra ATA 100 Interface, 1-FDD Interface, 4-PCI Slots, 1-PCI Express x16 slot, 1-PCI Express x1 Slot, 8-Digital I/O Lines and up to 4 GB DDR2 533/667 dual-channel SDRAM in 4-DDR2 DIMM Sockets

PROCESSOR: PENTIUM II

Diamond Systems Corporation

Website: www.diamondsystems.com
Model: Elektra **RSC No:** 23532

Two-in-one design reduces cost, saves space • ST VEGA Pentium-II class processor, 200 MHz, fanless • Integrated analog and digital I/O with autocalibration • 128 MB RAM soldered on board for increased ruggedness • 10/100 Mbps Ethernet • Four RS-232 serial ports • Two USB 1.1 ports with legacy USB floppy support • PS/2 keyboard and mouse • Programmable watchdog timer • -40 °C to +85 °C • PC/104 form factor • Works with Pandora cable-free enclosure system • Runs Linux, DOS, QNX, and Windows CE

PROCESSOR: POWERPC

Mercury Computer Systems, Inc.

Website: www.mc.com
Model: VPA-200 **RSC No:** 23651

VITA 41/VME single board computer • Dual 1.2 GHz MPC7448 processors • 2 GB of SDRAM • PCI Express or Serial RapidIO over P0 • 2eSST Support - More than 300 MBps • Two 33/66/133 MHz and 32/64-bit PMC slots • Two front-panel Gigabit Ethernet ports and RJ-11 serial ports

PROCESSOR: XSCALE

Applied Data Systems

Website: www.applieddata.net
Model: BitsyXb **RSC No:** 23628

Powerful embedded single board computer • Leverages Intel's 520 MHz XScale CPU, the Intel @ PXA270 • Variable speed and voltage regulation • Perfect for handheld, wearable, and unmanned applications • Compact, robust, ADSmart IO • Ruggedized and power-thrifty

Model: Portal **RSC No:** 23629

32-bit Intel XScale IXP 425 RISC processor @ 533 MHz • Incorporates SPI, 480 MB USB (high speed) • Dual Ethernet and/or 24-bit color SVGA graphics • Applications for military, digital signage, instrumentation, gaming, and others

SOFTWARE: OPERATING SYSTEM

CMX Systems, Inc.

Website: www.cmx.com
Model: CMX-RTX RTOS **RSC No:** 23602

Small ROM/RAM footprint • Royalty-free • Full source code proivded • Free technical support • Support for over 50 target processor families • Free software updates • Truly preemptive • Fast context switch times • Low interrupt latency periods • Kernel awareness for many debuggers • Additional TCP/IP or CANopen modules • Support for over 30 compiler manufacturers

MapuSoft Technologies

Website: www.mapusoft.com
Model: OS Abstractor/OS Changer **RSC No:** 23611

OS Abstractor product that gives users the ability to develop code independent of underlying OS • Will run on multiple operating systems including Nucleus PLUS, Precise/MQX, ThreadX, Linux, LynxOS OS, eCOS, Solaris, uITRON, Windows CE, and other Windows platforms • VxWorks OS Changer solutions are available to port from VxWorks to Nucleus PLUS, Precise/MQX, ThreadX, Linux, LynxOS, Solaris, eCOS, uITRON, Windows CE, and other Windows platforms • pSOS OS Changer solutions are available to port from pSOS to Nucleus PLUS, Precise/MQX, ThreadX, Linux, LynxOS, Solaris, eCOS, uITRON, Windows CE, and other Windows platforms • Nucleus OS Changer solutions are available to port from Nucleus to Linux, LynxOS, eCOS, Windows CE, and other Windows Platforms • POSIX OS Changer solutions are available to port POSIX code to various target operating systems • Royalty-free, full source code

SOFTWARE: PROTOCOL STACK

CMX Systems, Inc.

Website: www.cmx.com
Model: CMX TCP/IP **RSC No:** 23605

100% RFC compliant TCP/IP stack • Small ROM/RAM footprint • Run with or without an OS • Full source code • No royalties • Free technical support • Free software updates • Support for more than 25 target processors • Support for most popular Ethernet controllers • Support for BSD (Berkeley) sockets • Fast data throughput • Easy to learn and use

STRUCTURED ASIC

ChipX, Inc.

Website: www.chipx.com
Model: CX Family Structd ASICs **RSC No:** 23624

More than 44 structured ASIC slices from 5 V 0.6 μ through 0.13 μ • Built-in, industry standard, silicon proven USB 2.0 PHY and other IP • Fine grain X-Cell Structured ASIC architecture for best performance and density • Highly configurable SRAM blocks of 9 kB for excellent memory use efficiency • Single-port, dual-port, or FIFO configurations of SRAM blocks • Broad range of I/O pads that can be power, ground • I/Os can support LVTTL, LVCMOS, HSTL, SSTL (18/2/3), 840 MBps LVDS, PCI, PCI-X, XOSC, and double data rate • Output drive strengths of up to 16 mA • Up to 250 MHz maximum global operating frequency • Core operating voltage 1.2 V, 1.5 V, 1.8 V, 3.3 V, 5 V • Commercial and industrial-grade temperature libraries • Low-jitter PLLs with output frequency range of 10 MHz - 1 GHz and synthesizable DLLs with output frequency up to 500 MHz

TELEPHONY: GENERAL

GAO Research, Inc.

Website: www.gaoresearch.com
Model: G729AB **RSC No:** 23527

Compliant to ITU-T G.729 Annex A and Annex B standards • Fully optimized for Texas Instruments TMS320C5000 and TMS320C6000 family of DSPs • Fully optimized for Analog Devices Blackfin processor family • Other supported platforms: ADSP21xx, ARM9, CEVA Teak and TeakLite, Intel Xscale and Pentium processors, MIPS32 and MIPS64 cores, Freescale PowerPC, Renesas SuperH, and STMicroelectronics ST20 and ST40 cores

VIDEO: PROCESSOR

VMETRO

Website: www.vmetro.com
Model: CameraLink PMC **RSC No:** 23650

Supports base, medium, and full mode camera link implementations • Up to 85 MHz camera link clock rate • Up to two cameras in base mode, or one camera in medium or full mode • Two mini camera link interface connectors • The CAML-MOD3 captures digital video from one or two camera link cameras for processing directly within the PMC-FPGA03's Virtex-II Pro FPGA

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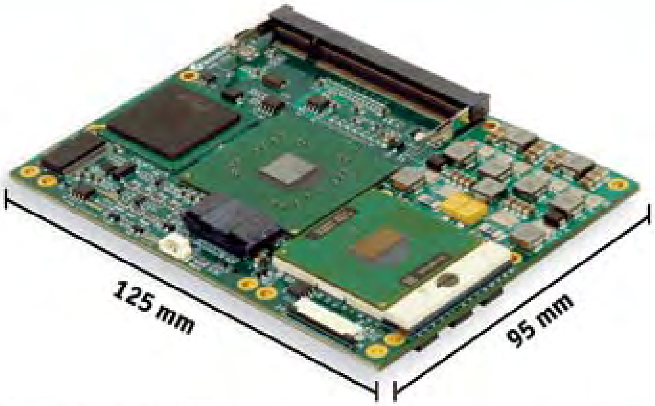

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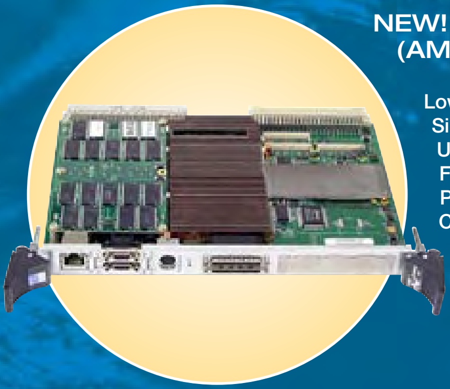

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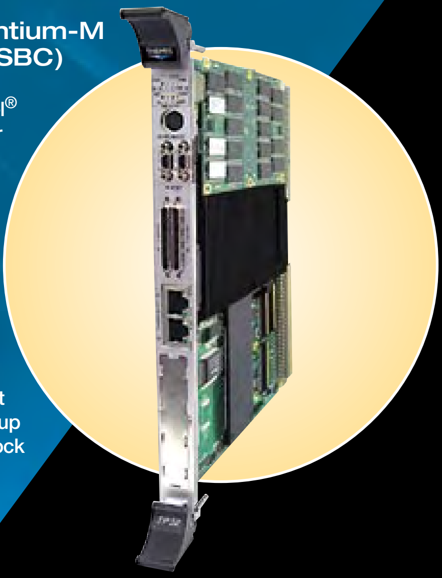

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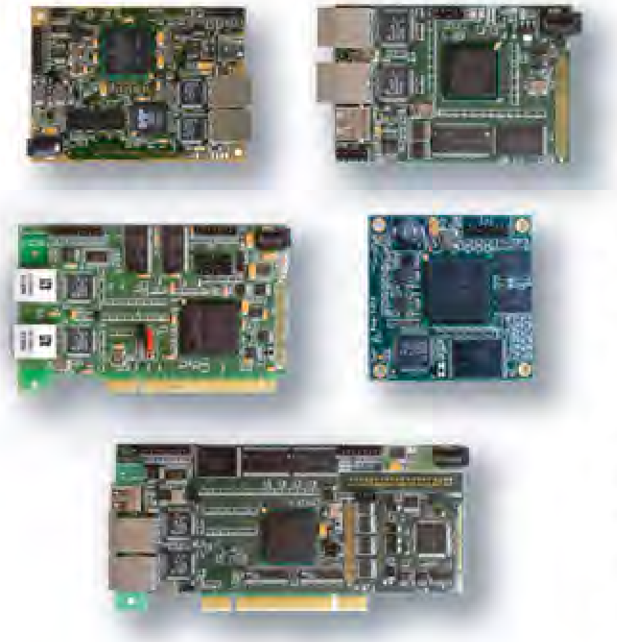

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